

## PI Optimized Cuckoo Search Algorithm for Single Phase Grid Tied PV Inverter with SEPIC Converter



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### ABSTRACT

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#### Keywords:

*PV system, SEPIC converter, MPPT algorithm, CS algorithm, DC-DC converter*

A new approach for single phase grid interconnected PV module with SEPIC converter is introduced in this paper. As the outcome of PV is low voltage DC, a suitable converter is needed to boost the voltage. Hence SEPIC converter is used as it has high voltage gain with same polarity in the input as well as output side. A closed loop control is executed with a PI controller tuned with Cuckoo search (CS) algorithm. As the traditional tuning of PI controller results in peak overshoot problems, Cuckoo search (CS) based Optimization is utilized as it is simple with has a smaller number of tuning parameters. This output is being fed to the grid through a single phase VSI and the grid synchronization is accomplished by PI controller by analogizing the actual and reference values of power. Thus, the proposed control strategy is verified through MATLAB and it is observed that the source current THD is minimized, which satisfies the IEEE standard.

## 1. INTRODUCTION

In the recent days, the Photo voltaic energy is widely utilized in all the countries and the Governments are trying to find more ways to satisfy the electrical requirements of the country with solar energy. Practically it is easier to implement and cost effective than other sources, which includes complex installation with highly expensive units of power generation; adding to that, this PV power is non-polluting and it requires less maintenance, because of which it is highly preferable in multiple structures. The photovoltaic power generators can be kept or installed at any place and the operation of PV is safe and quiet. In photo voltaic technique, the power is generated when the semiconductors material is hit by the sunlight. In the PV fed system, the input current with discontinuous operation and oscillatory output voltage have been gained with the effect of partial shading and highest ripple. A PV fed zeta converter is developed by evaluating the mathematical notations [1]. The MPPT algorithm is utilized for tracking the output power from the PV panel and this technique includes SEPIC converter with PWM for reducing the difficulty of the system [2]. A buck converter is developed with zeta, which includes inductors and capacitors by utilizing a sliding mode controller, the performance of which is compared with other converters [3]. For wind power generation, a synchronous generator with permanent magnet is linked with rectifiers. The reference voltage is made as constant with respect to the voltage in the open circuit of zeta converter yet maintaining a stable voltage is difficult [4]. Pazhampilly et al. [5] have discussed about the PV fed MPPT technique with incremental conductance feedback current and voltage. In consideration with various types of converters, MPPT is presented for extricating the power from PV system and the total output power of the system is comparatively lower than the other existing

techniques. In this works [6], a fuzzy logic controller (FLC) is utilized for the extraction of highest output power. The FLC has utilized the Mamdani's technique as the convergent and divergent membership function of PV system. A zeta converter is fed with PV array for MPPT [7]. The Researchers have evaluated the fuzzy logic controller, which utilizes the code tree format along with the P&O algorithm of MPPT tracking in the PV panel [8]. AC voltage is generated by utilizing a Zeta converter and the generated power is given to the 3-phase rectifier by providing the desired outputs [9]. BLDC motor with minimum switching losses including a tracking Algorithm is utilized [10]. P & O control technique is utilized for PV system with MPPT and a comparison is done between the SEPIC and BOOST converter [11]. A modified SEPIC converter is created for minimal switching voltage and high static gain, along with that, a modified SEPIC configuration is used through magnetic coupling to attain reduced input voltage performance [12].

A modified MPPT technique is utilized for SEPIC converter with fuzzy logic control for limiting the voltage variation [13-16]. A PV fed SEPIC converter is presented with fuzzy controller [17]. Fuzzy is used for maintaining the voltage as constant at various load conditions. A modified technique for solar PV voltage tracking is utilized with SEPIC converter. Incremental conductance technique is utilized for MPPT and implemented in MATLAB [18, 19]. The performance of the system with respect to THD & Output efficiency is differentiated by the converter [19]. Hence the desired output voltage is gained by setting the output voltage [20]. Though there are a number of developed methods and modified techniques, each of them has lacked in a certain criterion. Hence in this work, a single-phase PV integrated grid with SEPIC converter is analyzed, in which a closed loop control is executed by cuckoo search-based optimization thereby

retaining the link voltage. Grid synchronization is also accomplished by a PI controller.

The organization of the paper is as follows: the description of the proposed system is given in section 2 and in section 3, the analysis of the PV model; the proposed converter and its control algorithm are presented. The results and discussion of the proposed work are given under section 4, with the conclusion following in section 5.

## 2. PROPOSED SYSTEM

In this proposed work, the input voltage of the converter is fed from solar PV panel. The arrangement of PV fed grid connected system is shown in Figure 1. Conversion of DC-DC is highly recommended for attaining the required voltage from PV. As CUK and buck boost converters have led to stress in electrical components and ends up with failure in device or overheating. SEPIC converter is utilized here since it overcomes the mentioned disadvantages. The output of converter is given to single-phase inverter whose switches are controlled by PI controller. via suitable filter circuits, the inverter output is given to utility grid.

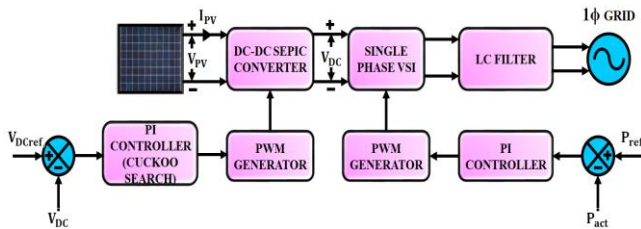


Figure 1. Proposed system block diagram

SEPIC has a distinctive operation i.e. the output voltage polarity is as similar as the input voltage polarity and the power has been transmitted from the input to output through the capacitor coupling. When converter is set in the on state due to coupling capacitor, L1 gets charged from the source whereas coupling capacitor gets decreased when the converter is set to off state. L1 is charged by the coupling capacitor and the energy, which has been transferred from L2 to output and diode is forward biased. SEPIC converter operates in two modes called continuous and discontinuous conduction modes. The current, which has been presented in the inductor is always higher than zero during continuous conduction mode while operating in full load; the total efficiency is always better. The current in the inductor is minimized to zero in Discontinuous conduction mode and remains in zero for specific switching cycle periods. It starts from zero and attains peak value then falls to zero if the duty cycle is high and thus the output is high. The output voltage of SEPIC is determined through duty cycle. It is capable of producing non inverted output by utilizing the coupling energy through series capacitor from input to output. SEPIC converter mainly focuses on frequency ripple suppression. It maximizes the total function of the system with minimal duty yield and maximum voltage gain in output. The efficacy of the converter has been maximized by utilizing CS Algorithm with MPPT technique. With the help of non-linear loads, reactive power is increased in the grid side. Due to non-linearity in grid characteristics, the current has become non-uniform so the quality of power is literally reduced and it affects the grid performance. Hence PI controller is utilized for the compensation in grid current and

the developed methodology attains maximum compensation in grid current. The developed methodology is a grid integrated technique without any storage system. SEPIC converter with Cuckoo Search Algorithm has increased the efficiency of the system by 96%. The circuit layout of this system is remarkably highlighted in Figure 2.

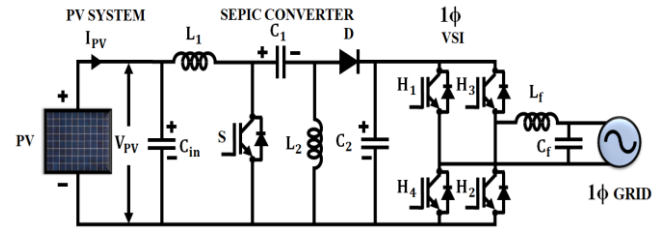


Figure 2. Proposed system circuit diagram

A 10 KHz triangular carrier and reference signal are differentiated, along with that, the pulses are fed to the SEPIC. In the developed technology, MPPT algorithm is utilized to attain stability in output voltage with lowest ripples, and the voltage source inverter is fed by the obtained voltage. The 1Φ VSI changes the DC into AC with pulsated output. Due to non-linearity in loads, the harmonics have been fed to the voltage and current, so the actual and reference power are analogized thereby the reactive power compensation, thus the PI based grid synchronization is accomplished.

## 3. ANALYSIS OF PROPOSED SYSTEM

### A) Modelling of PV Panel

A traditional PV system is presented in Figure 3.

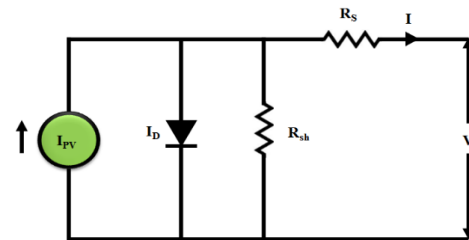


Figure 3. Model for one diode PV system

where, the PV current is denoted as  $I_{PV}$ , diode current is denoted as  $I_D$ , the resistance in series is denoted as  $R_s$ , the resistance in shunt is denoted as  $R_{sh}$ , the output current is denoted as  $I$  and the output of PV voltage is denoted as  $V$ .

Photo Voltaic panel current is given below;

$$I = I_{PV} - I_0 \left[ e^{\frac{(v+R_s I)}{V_k \alpha}} - 1 \right] - \frac{V + I R_s}{R_{sh}} \quad (1)$$

where,  $I_0$  represents PV saturation current,  $V_k$  represents the high thermal voltage and  $\alpha$  represents the ideality constant of diode.

Four Photo Voltaic panels are used in this proposed method. SEPIC converter is fed by the obtained photo voltaic output.

### B) SEPIC Converter

The input voltage can be increased or decreased through a

converter known as SEPIC Converter. This is basically a boost converter, in which the operation is differentiated in two modes. They are:

- CCM
- DCM

### CCM

In this mode, the current in the inductors  $L_1$  and  $L_2$  is constant and never drops to zero, which prevents the inductance from fully discharged.  $C_{in}$  is equal to that of  $V_{in}$  during the steady state operation of SEPIC converter and the current flowing through  $C_{in}$  is 0A. Output load is independent of  $V_{in}$  and is equivalent to the average current of  $L_2$ .

In CCM, sum of voltage across the energy storage element of SEPIC converter has been equivalent with input voltage (input and output filter capacitors  $C_{in}$  and  $C_o$  are excluded) which is given below,

$$V_{in} = V_{L1} + V_{Cin} + V_{L2} \quad (2)$$

Here the average voltage across  $C_{in}$  is same as  $V_{in}$ ,

$$V_{L1} = -V_{L2} \quad (3)$$

In steady state, CCM of SEPIC converter takes place in two ways based on the ON and OFF state of switch S. To study the function of SEPIC converter in CCM, it is essential to know the condition of switch S.

### ON state of switch S

Figure 4 explains the function of SEPIC converter in the ON state of switch S. In steady state, no current has been flowed through the filter capacitors  $C_{in}$  and  $C_o$  till they are discharged. Ripple in the SEPIC's converters input and output voltages becomes zero when the capacitance  $C_{in}$  and  $C_o$  are large.

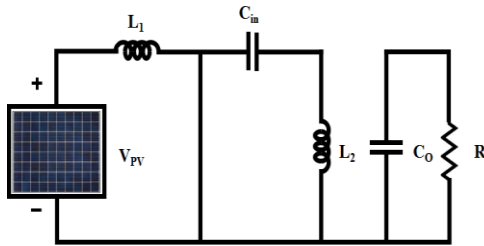


Figure 4. Switch on condition

During the first half-switching cycle i.e., in ON state, the current through  $L1$  and  $L2$  have increased both in positive and negative direction. Here  $L_1$  and  $L_2$  have charged and discharged through  $V_{in}$  and  $C_{in}$ . In the short period of time, the switch S remains closed, at this instant, the instantaneous voltage across  $C_{in}$  is equal to  $V_{in}$ .  $V_{L1}$  and  $V_{L2}$  are equal with magnitude  $V_{in}$ .

### OFF state of switch S

Figure 5 explains the operation of SEPIC when switch S is open or in OFF state.  $L_1$  and  $C_{in}$  are the new path for the input current. Inductor current has not changed immediately since the inductor  $L_1$  is equal to the capacitor current  $C_{in}$  and current  $L_2$  remains to discharge.  $C_o$  discharges in the half-switching cycle thus  $D$  turns on and supplies the current to the load.

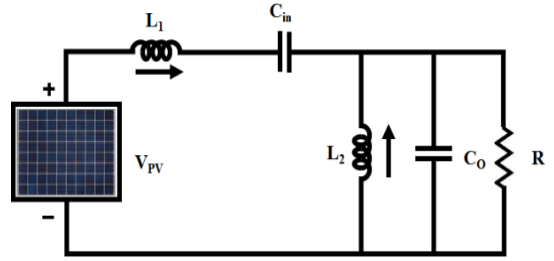


Figure 5. Switch off condition

Here, the input current is added by the current flows in the direction of  $L_2$ , which also flows to the output load that draws current from the inductance  $L_1$  and  $L_2$  when the switch S is in the OFF state.  $C_{in}$  is charged by  $V_{in}$  and  $L_1$  (when switch S conducts during half switching cycle is discharged), and to the next half switching cycle, the switch S conducts the current to the load output till  $L_2$  continues in discharging ( $L_2$  is charged by the current that is supplied by  $C_{in}$ ).

### DCM

The inductor current becomes zero in this mode of operation. For significant time period, the current through  $L_1$  and  $L_2$  remain at 0A. In less load current, it has maximum efficiency while operating this converter in DCM but needs more operating at maximum load current. Hence it yields more efficiency in this operation. SEPIC converter contains capacitance and Inductance, which aids to work in continuous mode with respect to the duty cycle in Eq. (4).

Duty Cycle:

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_{AN} + V_D} \quad (4)$$

where,  $V_{OUT}$  represents the output voltage,  $V_D$  represents the voltage across the diode and  $V_{IN}$  represents the input.

Inductor and capacitor output value has been given as,

$$L_1 = L_{2,3} = \frac{V_{IN} \times D_{max}}{I_1 \times f_s} \quad (5)$$

$$C_2 = \frac{I_o \times D_{max}}{V_{ripple} \times V_D \times f_s} \quad (6)$$

$I_o$  = Current output

$V_{ripple}$  = Voltage ripple

$D_{max}$  = Diode maximum value

$V_D$  = Voltage in Diode

$f_s$  = Switching frequency

Load Resistance is given as,

$$R = \frac{V_{out}}{I_{out}} \quad (7)$$

Here  $V_{out}$  and  $I_{out}$  represents the output Voltage and current respectively.

Current through the inductor is given as,

$$\Delta I_L = \frac{I_{out} \times V_o \times 40\%}{V_{IN}} \quad (8)$$

RMS current in the output capacitor is given as,

$$I_{out} (RMS) = I_{OUT} \times \sqrt{\frac{D_{max}}{1 - D_{max}}} \quad (9)$$

RMS current of coupling capacitor is given as,

$$I_{C1}(\text{RMS}) = I_{IN} \times \sqrt{\frac{D_{\max}}{1-D_{\max}}} \quad (10)$$

Voltage ripple of coupling capacitor  $C_1$  has been mentioned as,

$$\Delta V_{C1} = \frac{I_{OUT} \times D_{\max}}{C_1 \times F_S} \quad (11)$$

### C) Control Strategies for SEPIC converter

Proper control of SEPIC converter is vital and this is accomplished by CS algorithm, which results in uniform output voltage of the converter. A comparator is utilized for differentiating the actual and reference values of link voltage. The error signal is given to PI controller and by CS Algorithm, the control parameters are turned as fine. As a result, reference signal is generated by the controlled parameters and differentiated with the carrier wave. Owing to this, pulses are generated and fed to SEPIC converter.

#### Cuckoo search Algorithm

The Cuckoo Search (CS) algorithm is influenced through the breeding performance of cuckoos, which is introduced by Yang and Deb. An impressive aspect of certain cuckoo species is the parasitism of the brood. In the nests of other birds, female cuckoos lay their eggs, which looks the same or different. If the host bird finds out the egg, these alien eggs are killed or the nest is destroyed and a new one is established at anywhere. Cuckoos use various techniques namely mimicking the colors of host eggs, selects finest nest and improves the ability to imitate the call of host chick to maximize the feeding opportunities to rise the chance of producing a novel cuckoo and to decrease the possibility of the demolition of eggs by the host birds. The parasitism of cuckoo brood is listed below,

1. Every cuckoo puts single egg and randomly dumps it into the nests of another bird species.
2. The Finest nests has been taken for the next generation of high quality eggs.
3. The quantity of available host nests has been set and it is often possible for host bird to find the cuckoo's eggs and throw it out. The pseudo code for CSO is illustrated as follows:

#### Pseudo code for CSO

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Start
Objective function  $F(x)$ ,  $x = (x_1, \dots, \dots, x_n)^t$ .
Create the size of initial population  $n$ .
Host nests  $X_i = (i = 1, 2, \dots, n)$ .
While ( $t < \text{max. generation}$ ) / ( $\text{stop criterion}$ )
Attain a cuckoo randomly by levy flight.
Analyze its fitness value  $F_i$ .
Select a nest amidst  $n$  i.e.  $j$  randomly.
If ( $F_i > F_j$ )
Use instead of  $j$  by the novel value;
End
Abandoned the fraction ( $P_a$ ) of poor nests;
Additionally, built new ones;
Save nest with adequate solutions
Rank the solution and choose the best current
End While.

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Print the outputs  
Stop

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To efficiently hunt for a novel nest, the performance of cuckoos is related with Levy flights in CSA. Levy flights illustrate the method of random walks, which are defined by the phase lengths and followed a distribution of power law. The Levy flight is expressed as,

$$x_i^{g+1} = x_i^g + \alpha' \otimes \text{Levy}(\lambda') \quad (12)$$

where, the number of current generation is denoted as  $g$ , i.e.  $g = 1, 2, \dots, \text{max} - \text{cycle}$  and the number of pattern is denoted as  $i$ ,  $\alpha' > 0$  is the Levy flight's step size that controls the flight scale, entry-wise multiplication is denoted as  $\otimes$ , Levy supply includes endless changes with the endless mean, which is denoted as  $\text{Levy}(\lambda')$ .

$$\text{Levy}(\lambda') \sim s^{-\lambda'} \text{avec}(1 < \lambda' \leq 3) \quad (13)$$

where, the step size is denoted as  $s$ . Through the similar performance of a constant Levy supply, two generally dispersed stochastic random parameters have produced the transfer possibility to shift it from the current position to the next position. The generation of next nests is expressed as,

$$x_i^{g+1} = x_i^g + \text{stepsize} \cdot \text{randn} \quad (14)$$

where, the random value between zero and one has been denoted as  $\text{randn}$ . The step size is expressed as:

$$\text{stepsize} = \alpha' \cdot \text{step} \cdot (x_i - x_{\text{best}}) \quad (15)$$

where, the  $(x_i - x_{\text{best}})$  is the difference factor which is utilized to choose the apt results. The step factor has been expressed as,

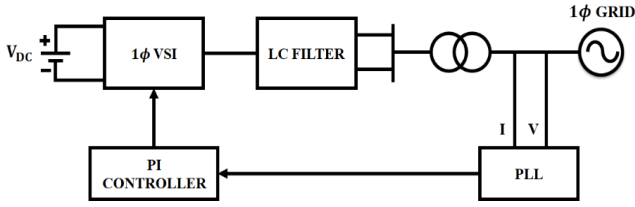
$$\text{step} = \left( \frac{\sigma(\lambda') \cdot \text{randn}}{\text{randn}} \right)^{\frac{1}{\lambda'}} \quad (16)$$

where, the standard deviation is denoted as  $\sigma$  and it is expressed as,

$$\sigma(\lambda') = \left( \frac{\Gamma(1 + \lambda') \cdot \sin(\pi\lambda'/2)}{\Gamma\left(\left(\frac{1 + \lambda'}{2}\right) \cdot \lambda' \cdot 2^{\frac{\lambda' - 2}{2}}\right)} \right)^{\frac{1}{\lambda'}} \quad (17)$$

The strength of the CS algorithm lies in how the solution space is manipulated and explored by a cuckoo. To find best solutions, this cuckoo has some 'intelligence'. The PI controller is tuned with CS algorithm and depending on the tuned parameters, the pulses for the SEPIC converter is generated with the aid of PWM generator.

The construction of 1 $\Phi$ DC link potential controller of PV inverter is given in Figure 6. The PV inverter voltage ( $V_{dc}$ ) has been given to LPF to minimize the ripples in switching. The filtered DC link potential and reference voltage ( $V_{dc}^*$ ) is given to PI to control the DC link voltage.



**Figure 6.** Grid synchronization by PI controller

The voltage error ( $V_{err}$ ) in  $n$ th sampling instant is given as,

$$\Delta v_{err}(n) = v_{dc}^*(n) - v_{dc}(n) \quad (18)$$

The output of PI at  $n$ th sampling time is,

$$i_{inv}^*(n) = i_{inv}^*(n-1) + K_{P1}(\Delta v_{err}(n) - \Delta v_{err}(n-1)) + K_{I1}\Delta v_{err}(n) \quad (19)$$

where, dc voltage controller proportionality is denoted as  $K_{P1}$ , and integral gain is denoted as  $K_{I1}$ . The reference currents have been generated with integrated grid potential for the PV inverter. Through this technique, PV inverter is highly proficient in generating the local load along with high current to reference value. When the requirement of load is greater than the production of PV, the grid has provided the necessitated currents.

The actual current in the inverter is compared with reference value in this mode of conduction. The output of PI has produced a change in the duty cycle ( $d$ ) and it is combined with the static duty ratio to generate the modulating signal.

#### 4. RESULTS AND DISCUSSION

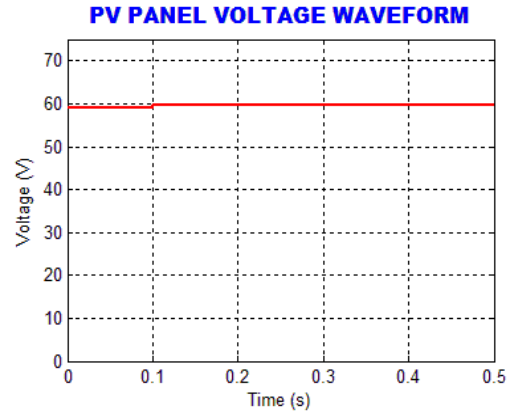
**Table 1.** Specifications for solar panel

COMPONENTS	RATINGS
Number of panels	3
Number of cells in series	36
Cell	125mm×31.25mm
OC voltage	21.4 V
Optimal operating voltage	16.8 V
SC current	1.21 A
Optimal operating current	1.19 A
Operating temperature	-40 to + 850C
Maximum system voltage	1000 VDC

**Table 2.** Specifications of SEPIC converter

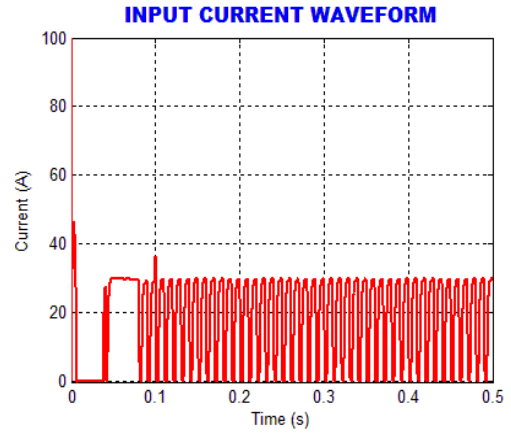
Components	Symbols	Rating
Input Voltage	$v_{in}$	0 to 100 V DC
Input Current	$i_i$	25 A (Max)
Capacitances	$C_1, C_2$	20 $\mu F$
Inductances	$L1, L2$	7 mH
Output load current	$I_L$	5 Amps
Switching frequency	$f$	10 KHZ
Output Power	$P_0$	700 W

A closed loop control of PV integrated grid with SEPIC converter by CS algorithm is analyzed by using MATLAB/SIMULINK. The voltage ratings of solar system and SEPIC Converter has been represented Tables 1 and 2. The simulated results have been highlighted and discussed in the following subsection.



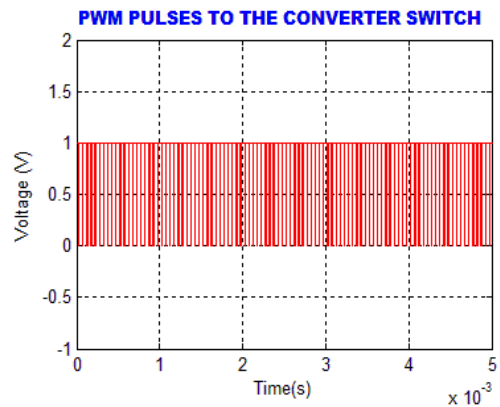
**Figure 7.** Simulated waveform of input DC voltage to SEPIC converter

The Figure 7 exhibits the SEPIC converter solar voltage. Owing to variation in solar panel input, output solar voltage has high ripples and that is given to the SEPIC.



**Figure 8.** Simulated waveform of input current from SEPIC converter

The Figure 8 presents the waveform of input inductor current in SEPIC converter,  $L1$  in SEPIC converter has controlled the input current as constant.



**Figure 9.** Simulated output of PWM pulse to SEPIC converter

The Figure 9 exhibits the PWM pulses for the SEPIC converter, which are generated by CS algorithm with switching frequency of 10 kHz. The CS algorithm is an

optimized self-tuning algorithm.

The Figure 10 exhibits the SEPIC converter output voltage by utilizing CS algorithm and it is observed that, comparatively CS algorithm provides more stability in voltage than MPPT algorithms [21].

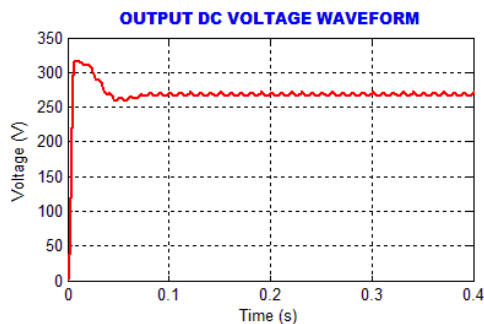


Figure 10. Simulated output voltage of SEPIC converter by utilizing CS algorithm

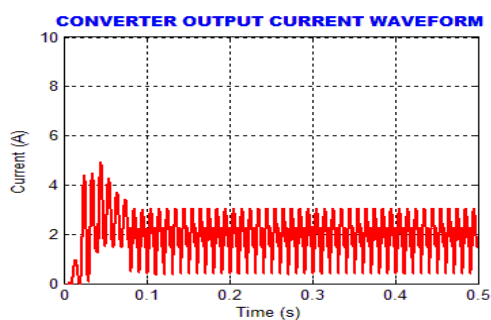


Figure 11. Simulated output DC current of SEPIC converter

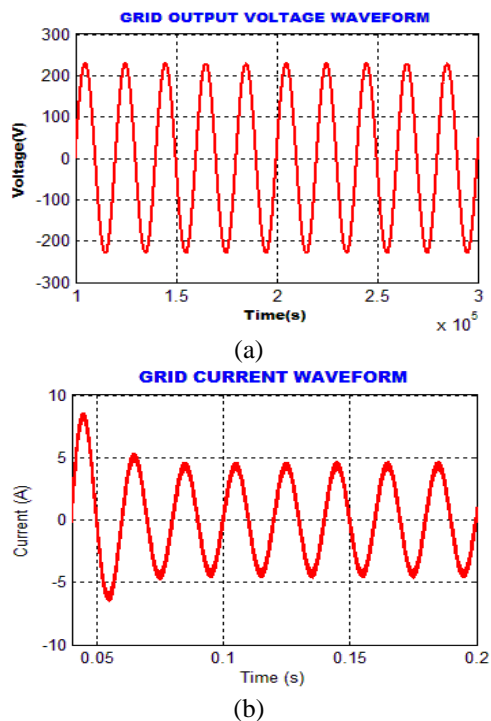


Figure 12. a Simulated waveform of grid voltage; b Simulated waveform Of Grid current

The Figure 11 exhibits SEPIC converter output current waveform, owing to noises in nonlinear load current.

The grid current compensation is accomplished by a PI controller. Figure 12.a and 12.b presents grid voltage and current waveforms correspondingly, which implies that both voltage and current are in phase i.e., unity power factor is attained. This presentation resembles a STATCOM device.

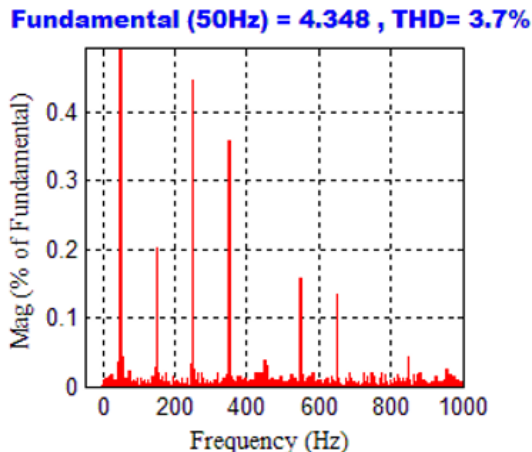


Figure 13. Simulated waveform of Current THD with CS algorithm

As represented in Figure 13, it is validated that the proposed single-phase grid tied PV system delivers a THD of 3.7%, which satisfy the IEEE standard.

## 5. CONCLUSIONS

PV based integrated grid with SEPIC has been explained in this work and the system's behavior is analyzed through MATLAB. A closed loop control is accomplished with a PI controller tuned with CS algorithm which provides minimum ripple with the aid of SEPIC. Through PI, the grid synchronization has been attained by comparing the reference and actual values of power thereby minimum THD is achieved. The power quality issues and standard theory levels of harmonics have been maintained by the inverter. The SEPIC with CS algorithm gives good performance than others, which has been validated through the simulated results. The proposed system is utilized in reactive power compensation and in the power grids.

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