

charge the UC, when its state of charge comes below half of its total capacity.

4. SIMULATION OUTCOMES

The simulation circuit of the proposed system is shown in Figure 6, and the simulation parameters are shown in Table. 1. The proposed system is designed and developed in Matlab / Simulink platform.

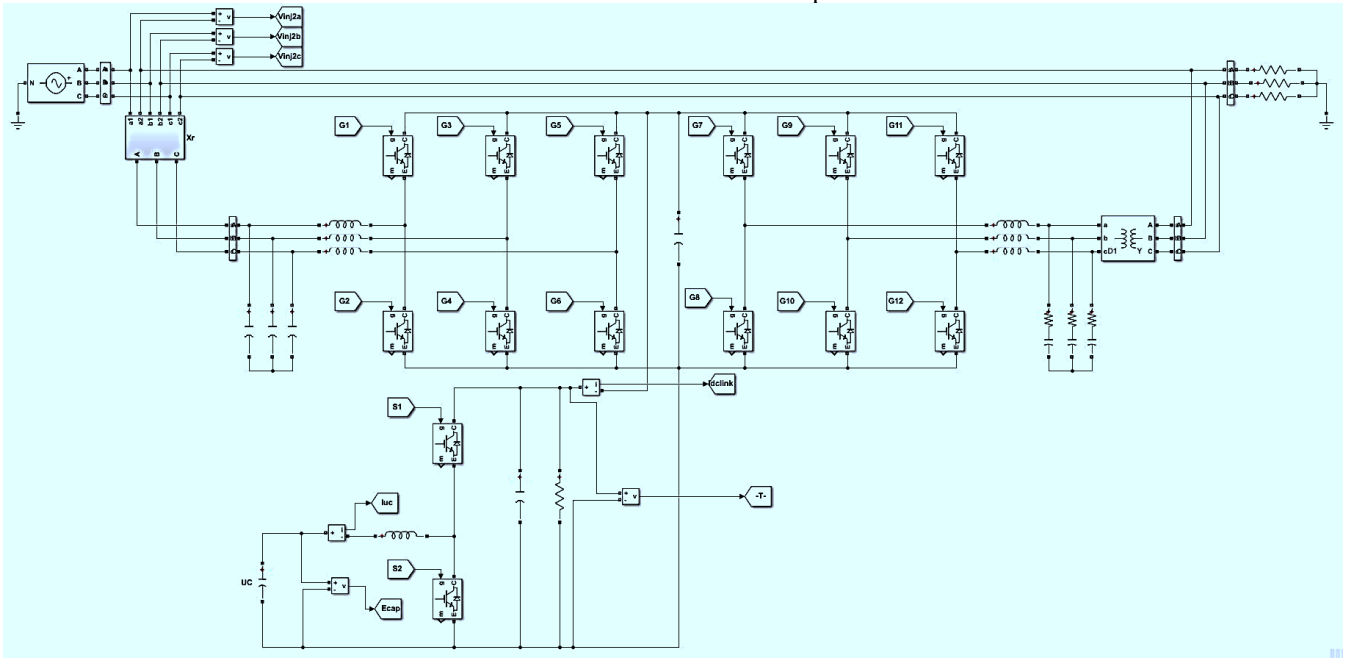
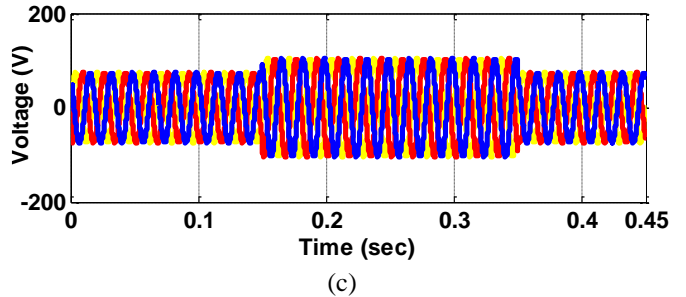
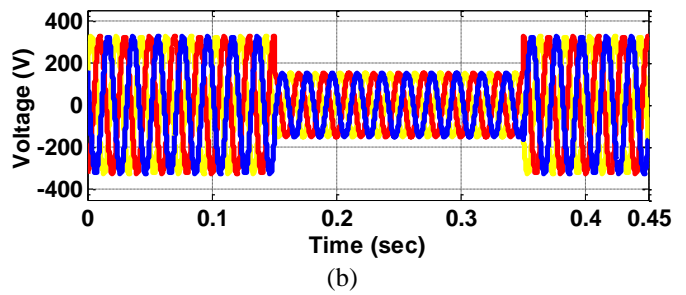
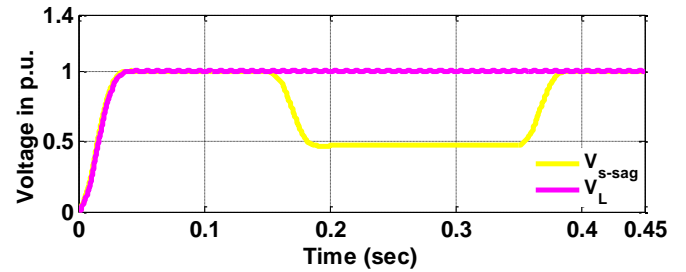


Figure 6. Simulation circuit of the proposed system.

Table 1. Simulation parameters of the proposed system.

Sl. No	Parameter	Value
1	DREGS/Grid Voltage, V_g	208 V
2	Capacitance of UC, C_{uc}	60 F
3	Input inductance of BDC, L_{BDC}	160 μ F
4	Output capacitance of BDC, C_{BDC}	45 μ F
5	Output resistance of BDC, R_{out}	215 Ω
6	DC link capacitance, $C_{dc-link}$	3600 μ F
7	DVR series inductance, L_{DVR}	1.5 mH
8	APF series inductance, L_{APF}	1.5 mH
9	DVR shunt capacitance, C_{DVR}	100 μ F
10	APF shunt capacitance, C_{APF}	100 μ F
11	Frequency	50 Hz

For the case I, the proposed system response is obtained in per unit values as shown in Figure 7(a), and for obtaining the three-phase system response the sag voltage of source in rms (V_{s-sag}) is induced in the system from time, $t = 0.15$ sec to 0.35 sec and the extent of the sag is taken up to 0.47 p.u. During sag, the load voltage (V_L) will be remained constant at around 0.99 p.u. with the help of UPQC. The line-to-line source voltages ($V_{sRY}, V_{sYB}, V_{sBR}$) of DREGS/grid is shown in Figure 7(b) and is having a voltage dip from 0.15 sec to 0.35 sec. This voltage dip is compensated by using a UPQC device with the help of UC-BDC, the injected voltages ($V_{inj2R}, V_{inj2Y}, V_{inj2B}$) is shown in Figure 7(c). During V_{s-sag} , the additional voltage required by the load is supplied by the UPQC to keep the line-to-line Load voltages ($V_{LRY}, V_{LYB}, V_{LBR}$) as constant as shown in Figure 7(d).



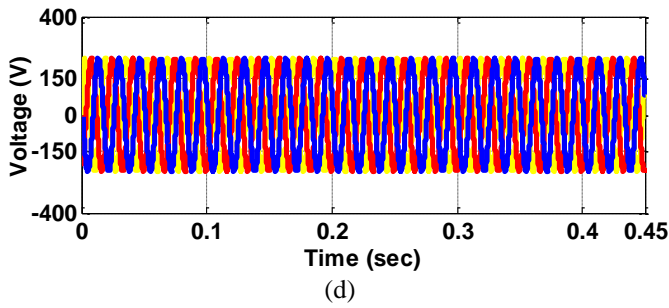
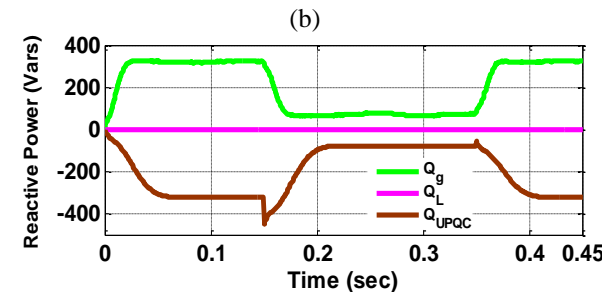
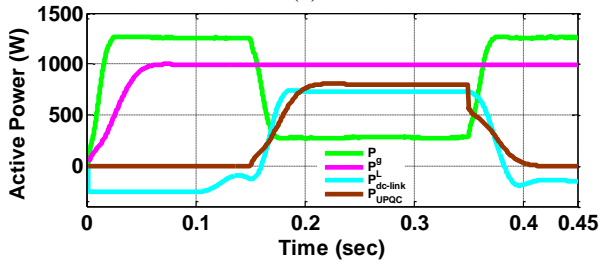
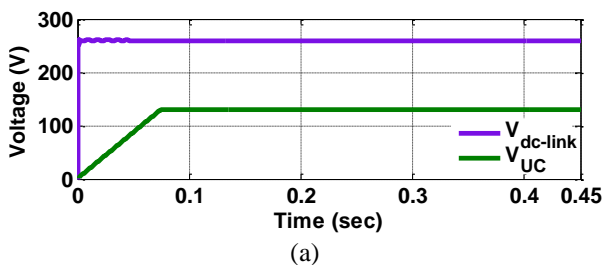


Figure 7. Voltage sag condition is taken from 0.15 sec to 0.35 sec (a) V_{s-sag} and V_L in p.u. (b) the line to line source voltages (c) injected voltages of UPQC (d) line to line load voltages.

During voltage sag, Figure 8(a) presents the voltage of a BDC, Figure 8(b) and Figure 8(c) presents the real and reactive powers of the DREGS/grid, load, and UPQC. From Figure 8, during voltage sag, the real power deficit from the DREGS/grid is compensated by the UPQC device, which is the same as the input power of the inverter which was taken from UC storage. It is also identified that during sag the reactive power from DREGS/grid is reduced and it is compensated using reactive power supplied by the UPQC. The proposed system's real and reactive power support is simulated using Figure 8. During the time, $t = 0$ to 0.225 sec, the system operates in reactive power assist mode using reactive power from the UPQC which is shown in Figure 8(c), from 0.225 sec to 0.45 sec, the system operates in real power assist mode. The voltages of UC and the dc-link side are shown in Figure 8(a) and the real and reactive powers of the proposed system are shown in Figure 8(b) and Figure 8(c).



(c)

Figure 8. Sag condition. (a) Voltages of BDC and UC. (b) Real and Reactive powers of the proposed system using UPQC.

For case II, the proposed system response is obtained in per unit values as shown in Figure 9(a), and for obtaining the three-phase system response the swell voltage of source in rms ($V_{s-swell}$) is induced in the system from time, $t = 0.15$ sec to 0.35 sec and the extent of the swell is taken up to 0.53 p.u. During sag, the load voltage (V_L) will be remained constant at around 0.99 p.u. with the help of UPQC. The line-to-line source voltages ($V_{SRY}, V_{SYB}, V_{SBR}$) of DREGS/grid is shown in Figure 9(b) and is having voltage dip from 0.15 sec to 0.35 sec. This voltage dip is compensated by using a UPQC device with the help of UC-BDC, the injected voltages ($V_{inj2R}, V_{inj2Y}, V_{inj2B}$) is shown in Figure 9(c). During V_{s-sag} , the additional voltage required by the load is supplied by the UPQC to keep the line-to-line Load voltages ($V_{LRY}, V_{LYB}, V_{LBR}$) as constant as shown in Figure 9(d).

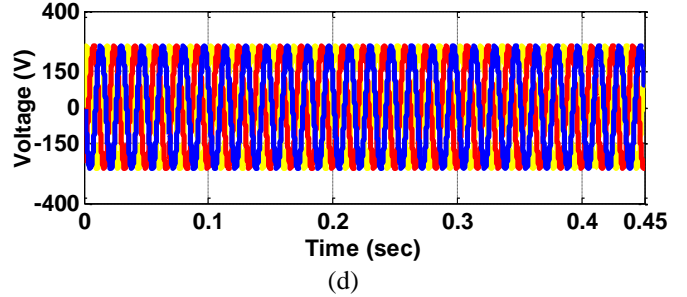
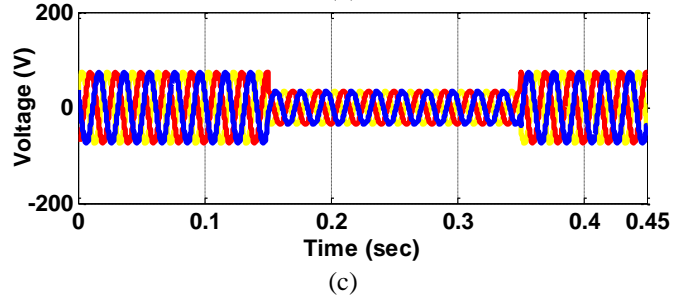
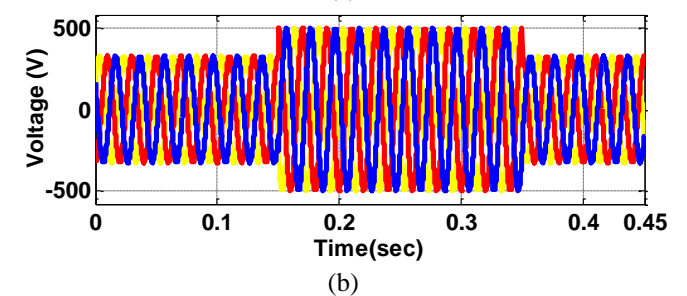
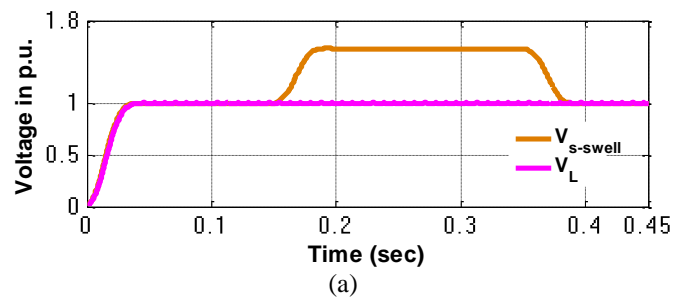


Figure 9. Voltage swell condition is taken from 0.15 sec to 0.35 sec. (a) $V_{s-swell}$ and V_L in p.u. (b) the line to line source voltages (c) injected voltages of UPQC (d) line to line load voltages.

During voltage swell, Figure 10(a) presents the voltage of a BDC, Figure 10(b) and Figure 10(c) presents the real and reactive powers of the DREGS/grid, load, and UPQC. From Figure 10, during voltage swell the surplus real power from the DREGS/grid is taken by the UPQC device, to charge the UC storage. The proposed system's real and reactive power are shown in Figure 10. The voltages of UC and the dc-link side are shown in Figure 10(a) and the real and reactive powers of the proposed system are shown in Figure 10(b) and Figure 10(c).

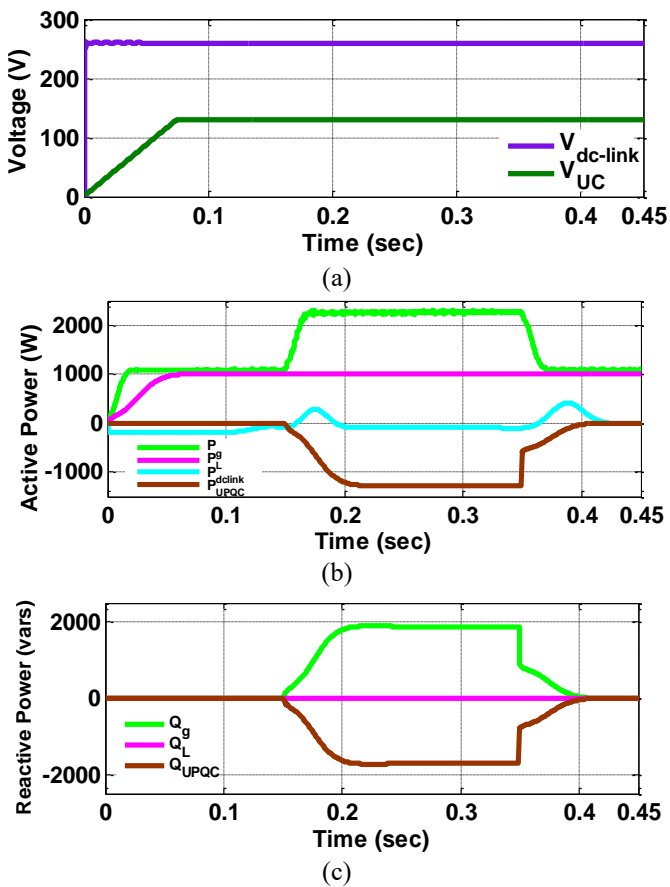


Figure 10. Swell condition. (a) Voltages of BDC and UC. (b) Real and Reactive powers of the proposed system using UPQC.

5. CONCLUSION

In this article, the proposed system uses an ultracapacitor based BDC converter and UPQC between the DREGS and loads to improve the power quality in the MG system. The voltage sag and swell will be compensated using the DVR portion of the UPQC. The real and reactive power assist will be provided by the APF portion of the UPQC to overcome the intermittencies caused by the disturbances. A CLIC integrated ACM control is employed to regulate the BDC converter to maintain the constant dc-link voltage. The DVR inverter employs an in-phase compensation control technique and the APF uses a current control d-q technique to control the proposed system are discussed. From the simulation results, it is clear that the proposed system performs well to compensate for the short-term disturbances in the Microgrids.

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