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# Pulse Width Modulation Technique for Multilevel Operation of Five-Phase Dual Voltage Source Inverters

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*five-phase voltage source inverter, multilevel inverters, space vector pulse width modulation, total harmonic distortion*

**ABSTRACT**

To supply five-phase variable speed drives, five-phase voltage source inverters are used. Some of the applications of five-phase variable speed drives are traction, electric & hybrid-electric vehicles, and ship propulsion. Different control systems are available for the controlled output of the five-phase VSI, but space vector pulse width modulation is popular because of its simpler digital implementation. In this paper, the SVPWM schemes have proposed and analyzed for the multilevel operation of a five-phase dual voltage source inverter. The proposed techniques do not contribute a voltage balancing issues such as in multilevel neutral point clamped (NPC) inverters. The author analyzed the performance of five-phase VSI based on THD and fundamental components. Matlab/Simulink model has provided for results verification.

## 1. INTRODUCTION

In the various industrial applications as traction, electric & hybrid-electric vehicles, and ship propulsion, variable speed AC drives are required. Usually, the three-phase machine is using to get the controlled output for this purpose but has some limitations in terms of power. To overcome these limitations in terms of more power, researches are going on more than three-phase i.e. polyphase machine. Polyphase machines have lots of advantages over three-phase like less volume to weight ratio, lower dc-link current harmonics, reducing rotor current harmonics, better noise, vibration characteristics, and many more. The detail description of these advantages is mentioned in the Refs. [1, 2]. The first five-phase induction motor i.e. first step in the polyphase machine has investigated in 1969 [3]. One of the main differences between three-phase and five-phase machine is that three-phase machines have a single stator current component across the d-q axis whereas five-phase machines have more than one stator current component as the axis increases [4, 5]. Due to an increase in additional component, generated torque is also increasing. This property makes the five-phase system very different from the three-phase system.

A system that can provide a controlled five-phase output supply, i.e. a five-phase inverter, is needed for powering the five-phase induction motor. This inverter input is a dc source, and the output is a controlled voltage and the frequency five-phase AC. Various control schemes are available for controlling the output of five-phase VSI, but the space vector pulse width modulation scheme is very common because of its advantages and easy digital implementation. A detailed overview of the SVPWM for the five-phase system can be found in the literature [5-9].

Researchers are also focusing on multilevel inverters. The multilevel term defines more than two-level whose performance is better than the two-level inverter because of lesser harmonics, electromagnetic interference, and higher dc-link voltages. The multilevel inverter is applicable for high voltage applications whereas two-level inverter has limitations. The benefits and the various topologies utilized in multilevel converters are elaborated in detail in the Refs. [10, 11]. Multilevel converters have many benefits, but they also have some drawbacks e.g., cost and circuit complexity increase as the output level increases.

In this article, the author discusses the five-phase two-level dual voltage source inverter. The author also proposes two controlling schemes for multilevel operation using space vector pulse width modulation for a five-phase two-level dual VSI. The author presented the vector diagram, switching table, switching waveform using two neighbouring large space vectors only then by using a combined application of medium and large space vectors. Here the objective is to preset the multilevel operation for five phase using two-level dual inverter system to minimize the complexity along with the cost of multilevel converters. In last results are verified in Simulink environment.

## 2. SPACE VECTOR PULSE WIDTH MODULATION IN DUAL-INVERTER SYSTEMS

Space vector pulse width modulation (SVPWM) is a technique used to determine the pulse-width modulated signals for the inverter switches in order to generate the desired phase voltages to the motor. The realization of SVPWM is based on proper selection of switching states of inverter in stationary reference frame and calculation of appropriate switching time periods [12].

An efficient PWM using a space vector method has been described to control the performance of split-phase induction

motor operation using a dual voltage source inverter, which also helps to eliminate fifth and seventh harmonics in the output voltage of the motor [13]. For a dual two-level VSI fed open-end winding, voltage space phasor fluctuations and zero sequence currents elimination have been presented in literature [14]. The least number of switches for each inverter, for the output voltage control has been presented Shivakumar et al. [15] and to reduce the switching for the duration of the changeover of inverters from switching to clamping and vice versa has presented in Mohan et al. [16]. In order to minimize neutral point fluctuations, zero sequence currents, and suppress triple harmonic currents, the open-end winding induction motor switching scheme was presented by Somasekhar et al. [17, 18]. A switching scheme has been presented by Kalaiselvi et al. [19] without using sector identification and lookup tables and to eliminate the common-mode voltage, and reduce the current ripple and decrease the total switching in both inverters [20]. A unified SVPWM scheme for dual voltage source inverters has been presented by Chen and Sun [21], and this has become the basis for the proposed schemes in this paper. In the proposed scheme, inverter system having two different dc voltage sources to minimize the total switching frequency and to provide the region identification for each sector.

## 3. MULTI-LEVEL MULTIPHASE: A REVIEW

Analysis and simulation were performed on a five-phase multi-level inverter using a carrier-based PWM with imbalance conditions on the induction machine [22], and the comparative simulation study was given by Jyothi and Rao [23] for a five-phase two-level and three-level inverter based on output efficiency. A phase opposition disposition (POD) and in phase disposition (IPD) control system comparison was analyzed for the control of the THD in output voltage and current for three-level five-phase inverters [24]. A new switch ladder topology has been presented to evaluate the performance level using symmetric and asymmetric sources for five-phase multilevel inverter drive [25, 26]. For three-stage t-type neutral point clamped (NPC), three-phase inverters using SVPWM [27], and three level NPC five-phase inverters, simulation and experimental analysis have been presented to minimize the typical mode voltage using redundant switching state voltage vectors [28]. The NPC inverter and the cascaded inverter topology were discussed to reduce the bearing current and common-mode voltage in the five-phase multilevel inverter [29]. The complexity of the power circuit and the cost of multilevel converters increase as the output level increases. The switch numbers in the two-level dual inverter and three-level single inverter system are the same, but the topology used in the three-level single inverter system needed additional voltage balancing capacitors and diodes. By using a dual inverter system, which does not need any additional diodes and capacitors, this condition can be resolved, and output ripples are greatly reduced [30]. This technique also simplifies the identification of regions in sectors and reduces the overall switching frequency.

## 4. DUAL TWO LEVEL FIVE-PHASE VOLTAGE SOURCE INVERTER AND PROPOSED SPACE VECTOR PWM

A power circuit diagram of a five-phase two-level dual VSI is shown in Figure 1 for three-level operation. Here is a positive end converter (blue inverter) referred to as INV 1 and a negative end converter (green inverter) referred to as INV 2. Five legs are composed in each inverter having two semiconductor switches in each leg i.e. IGBT, totaling ten switches. The operation of both switches on the same leg is complementary, to avoid the short-circuiting of the input DC source. The inverters' inputs are supplied with equal/unequal values from isolated dc-link sources and the outputs are connected to the open-end winding.

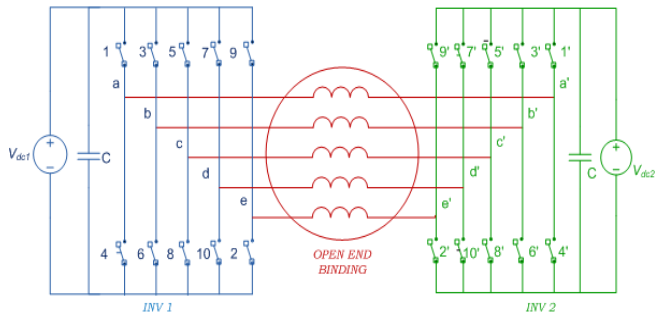


**Figure 1.** Circuit diagram of five phase two-level dual voltage source inverter

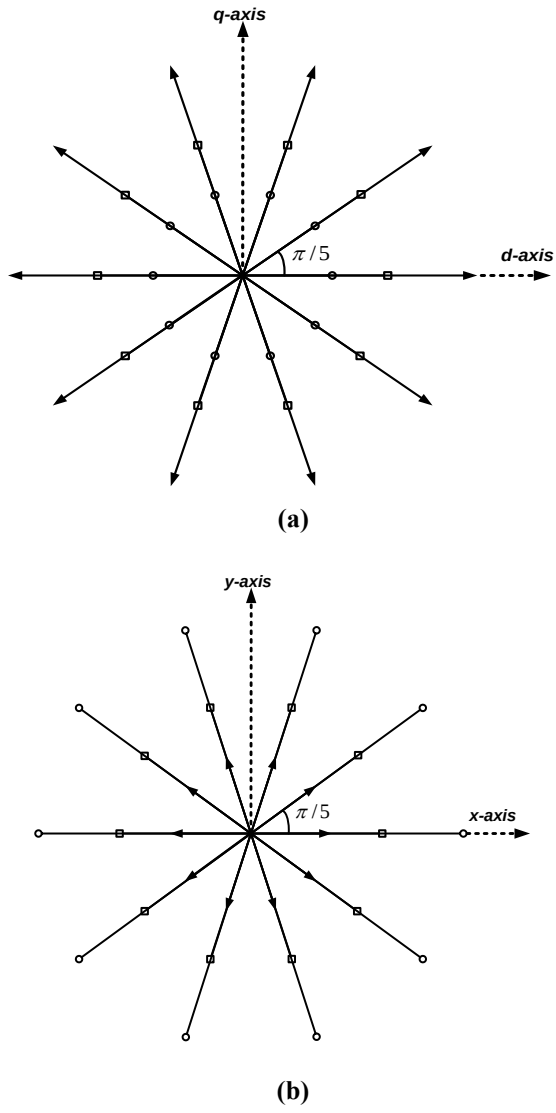


**Figure 2. (a)** Phase voltage space vector *d-q* plane; **(b)** Phase voltage space vectors in *x-y* plane

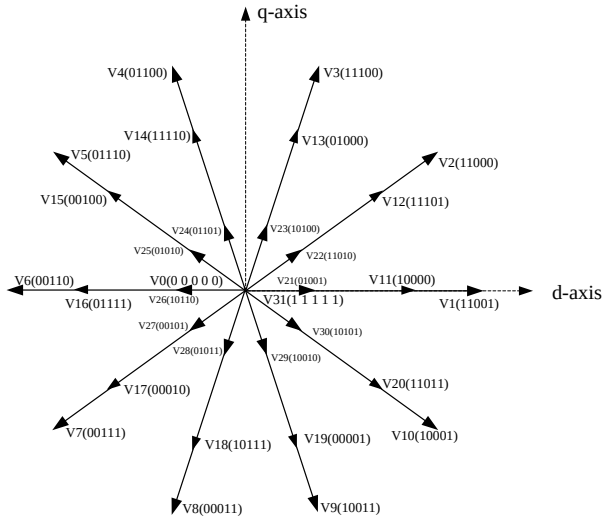


**Figure 3.** Voltage vector plane and voltage selection for dual inverter

Using the SVPWM scheme, each inverter in a five-phase system has thirty-two switching vectors with thirty active vectors and two zero vectors [5]. The five-phase input voltage and space vector equation are given using power invariant matrix:

$$\begin{aligned} v_a &= \sqrt{2}V\cos(\omega t) \\ v_b &= \sqrt{2}V\cos(\omega t - 2\pi/5) \\ v_c &= \sqrt{2}V\cos(\omega t - 4\pi/5) \\ v_d &= \sqrt{2}V\cos(\omega t + 4\pi/5) \\ v_e &= \sqrt{2}V\cos(\omega t + 2\pi/5) \end{aligned} \quad (1)$$

$$\underline{v}_{dq} = \frac{2}{5}(v_a + \underline{a}v_b + \underline{a}^2 v_c + \underline{a}^{*2} v_d + \underline{a}^* v_e) \quad (2a)$$

$$\underline{v}_{xy} = \frac{2}{5}(v_a + \underline{a}^2 v_b + \underline{a}^* v_c + \underline{a}\, v_d + \underline{a}^{*2} v_e) \quad (2b)$$

where, $\underline{a} = \exp(j2\pi/5)$, $\underline{a}^2 = \exp(j4\pi/5)$, $\underline{a}^* = \exp(-j2\pi/5)$, $\underline{a}^{*2} = \exp(-j4\pi/5)$ and * stands for a complex conjugate. The phase voltage space vectors thus obtained in *d-q* plane using (2a) are shown in Figure 2 and since it is a five-phase system, transformation is further done to obtain space vectors in *x-y* plane using (2b) and the resulting space vectors are shown in Figure 3.

All the thirty active vectors have divided in three groups according to their magnitude i.e. large vectors, medium vectors and small vectors. The author has proposed two PWM schemes for the five-phase dual VSI (a) using only large vectors (b) using large and medium vectors.

The selection of switching voltage for the dual inverter having two different dc voltage sources is illustrated in Figure 3.

### 4.1 Using only large voltage vectors

For the generation of reference voltage vector, two neighboring large active voltage vectors, and one null voltage vector is used for every inverter [30]. The duration of time of both the active space voltage vector has presented by

$$T_1 = \frac{|\underline{v}_{ref}|\sin(k\pi/5 - \alpha)}{|\underline{v}_l|\sin(\pi/5)} T_s \quad (3)$$

$$T_2 = \frac{|\underline{v}_{ref}|\sin(\alpha - (k-1)\pi/5)}{|\underline{v}_l|\sin(\pi/5)} T_s \quad (4)$$

$$T_0 = T_s - T_1 - T_2 \quad (5)$$

Here symbol, k = sector number (k= 1 to 10 for five phase), $|\underline{v}_l| = \frac{2}{5}V_{dc}2\cos(\pi/5)$ = peak of length of large voltage vector, $\underline{v}_{ref}$ = reference vector, l = large space vectors, $T_s$ = sampling period and $\theta(0, \pi/5)$ = angle between $V_{ref}$ & $V_1$.

**Table 1.** Switching sequence for the multi-level operation

| Sector | Switching Sequence | | | | | | |
|---|---|---|---|---|---|---|---|
| **I** | V0 | V2 | V1 | V0 | V1 | V2 | V0 |
| | 00000 | 11000 | 11001 | 11111 | 11001 | 11000 | 00000 |
| **II** | V0 | V2 | V3 | V0 | V3 | V2 | V0 |
| | 00000 | 11000 | 11100 | 11111 | 11100 | 11000 | 00000 |
| **III** | V0 | V4 | V3 | V0 | V3 | V4 | V0 |
| | 00000 | 01100 | 11100 | 11111 | 11100 | 01100 | 00000 |
| **IV** | V0 | V4 | V5 | V0 | V5 | V4 | V0 |
| | 00000 | 01100 | 01110 | 11111 | 01110 | 01100 | 00000 |
| **V** | V0 | V6 | V5 | V0 | V5 | V6 | V0 |
| | 00000 | 00110 | 01110 | 11111 | 01110 | 10110 | 00000 |
| **VI** | V0 | V6 | V7 | V0 | V7 | V6 | V0 |
| | 00000 | 00110 | 00111 | 11111 | 00111 | 10110 | 00000 |
| **VII** | V0 | V8 | V7 | V0 | V7 | V8 | V0 |
| | 00000 | 00011 | 00111 | 11111 | 00111 | 00011 | 00000 |
| **VIII** | V0 | V8 | V9 | V0 | V9 | V8 | V0 |
| | 00000 | 00011 | 10011 | 11111 | 10011 | 00011 | 00000 |
| **IX** | V0 | V10 | V9 | V0 | V9 | V10 | V0 |
| | 00000 | 10001 | 10011 | 11111 | 10011 | 10001 | 00000 |
| **X** | V0 | V10 | V1 | V0 | V1 | V10 | V0 |
| | 00000 | 10001 | 11001 | 11111 | 11001 | 10001 | 00000 |

During sampling time, two reference voltages generated by both the inverters are used to generate the average voltage vector. Using the proposed method, dual two-level five-phase VSI inverter performance is similar to multilevel operation as in a multi-level neutral point clamped (NPC) inverter. Another advantage of this scheme is that, along with minimizing switching losses, it minimizes the overall total harmonic distortion, the switching pattern for multilevel operations is shown in Table 1.

During the synthesis process both the reference voltages Vref & Vref' produced by each inverter move in all the ten sectors (I to X) in decagon vector diagram using ten active vectors for INV 1($V_1$ to $V_{10}$) and ten active vectors for INV 2 ($V_{1'}$ to $V_{10'}$) and two null vectors ($V_0$&$V_{0'}$) positioned at origin. It is a key feature to reduce the switching losses, switching, and overall THD for inverter function. The switching waveform for dual VSI for both reference voltages (Vref & Vref') are in Figure 4(a). For greater comprehension switching pattern is presented in blue for INV 1 and green for INV 2 utilizing space vector $V_0$, $V_1$, $V_2$, $V_0$', $V_{8'}$, and $V_9$' and line voltages are presented in black color during the sampling period.

### 4.2 Using large and medium voltage vectors

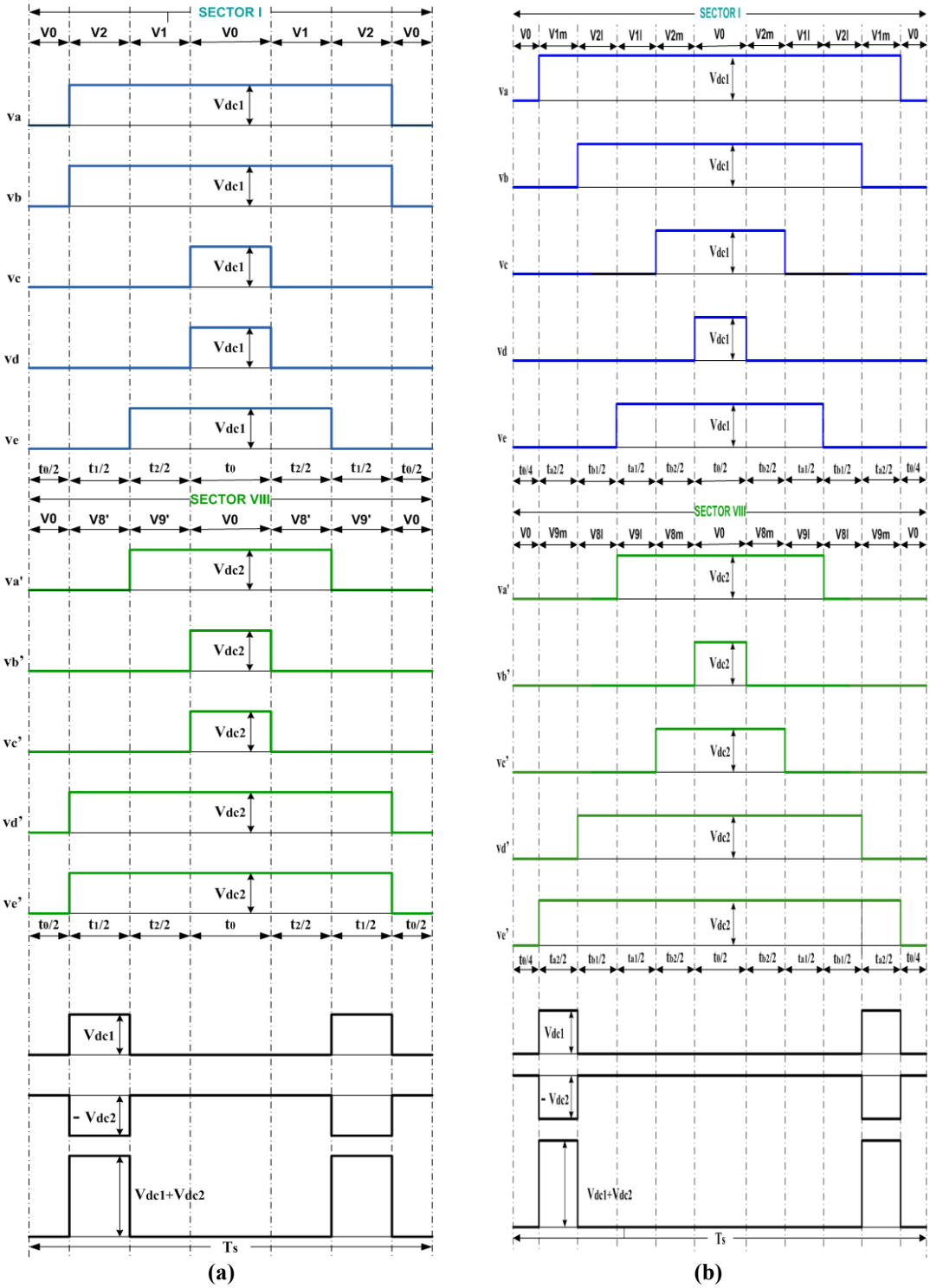


**Figure 4. (a).** Switching waveforms for five phase two-level dual VSI for multilevel operation using large vectors only; **(b).** Switching waveforms for five phase two-level dual VSI for multilevel operation using large and medium vectors

**Table 2.** Switching sequence for the multilevel operation using large and medium vector

| Sector | Switching Sequence | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **I** | V0 | V1 | V2 | V1 | V2 | V0 | V2 | V1 | V2 | V1 | V0 |
| | 00000 | 10000 | 11000 | 11001 | 11101 | 11111 | 11101 | 11001 | 11000 | 10000 | 00000 |
| **II** | V0 | V3 | V2 | V3 | V2 | V0 | V2 | V3 | V2 | V3 | V0 |
| | 00000 | 01000 | 11000 | 11100 | 11101 | 11111 | 11101 | 11100 | 11000 | 01000 | 00000 |
| **III** | V0 | V3 | V4 | V3 | V4 | V0 | V4 | V3 | V4 | V3 | V0 |
| | 00000 | 01000 | 01100 | 11100 | 11110 | 11111 | 11110 | 11100 | 01100 | 01000 | 00000 |
| **IV** | V0 | V5 | V4 | V5 | V4 | V0 | V4 | V5 | V4 | V5 | V0 |
| | 00000 | 00100 | 01100 | 01110 | 11110 | 11111 | 11110 | 01110 | 01100 | 00100 | 00000 |
| **V** | V0 | V5 | V6 | V5 | V6 | V0 | V6 | V5 | V6 | V5 | V0 |
| | 00000 | 00100 | 00110 | 01110 | 01111 | 11111 | 01111 | 01110 | 10110 | 00100 | 00000 |
| **VI** | V0 | V7 | V6 | V7 | V6 | V0 | V6 | V7 | V6 | V7 | V0 |
| | 00000 | 00010 | 00110 | 00111 | 01111 | 11111 | 01111 | 00111 | 10110 | 00010 | 00000 |
| **VII** | V0 | V7 | V8 | V7 | V8 | V0 | V8 | V7 | V8 | V7 | V0 |
| | 00000 | 00010 | 00011 | 00111 | 10111 | 11111 | 10111 | 00111 | 00011 | 00010 | 00000 |
| **VIII** | V0 | V9 | V8 | V9 | V8 | V0 | V8 | V9 | V8 | V9 | V0 |
| | 00000 | 00001 | 00011 | 10011 | 10111 | 11111 | 10111 | 10011 | 00011 | 00001 | 00000 |
| **IX** | V0 | V9 | V10 | V9 | V10 | V0 | V10 | V9 | V10 | V9 | V0 |
| | 00000 | 00001 | 10001 | 10011 | 11011 | 11111 | 11011 | 10011 | 10001 | 00001 | 00000 |
| **X** | V0 | V1 | V10 | V1 | V10 | V0 | V10 | V1 | V10 | V1 | V0 |
| | 00000 | 10000 | 10001 | 11001 | 11011 | 11111 | 11011 | 11001 | 10001 | 10000 | 00000 |

The harmonic content is present in the output phase voltages using only large voltage vectors. This implies that, as only two active vectors are often used in each sector, we do not get satisfactory results. For a pure sinusoidal voltage waveform, the number of vectors should be one less than the number of phases [30]. This means that four active voltage vectors should be used rather than two to achieve satisfactory sinusoidal outcomes in a five-phase system. For each inverter, two neighboring large and two neighboring medium active voltage vectors are used for the generation of reference voltage vectors along with one null voltage vector. The switching waveform for dual VSI for both reference voltages (Vref & Vref') using large and medium vectors are in Figure 4(b). The duration of time of both the active space voltage vector has presented by:

$$T_{al} = \frac{|\underline{v}_l|}{|\underline{v}_l| + |\underline{v}_m|} T_a$$

$$T_{bl} = \frac{|\underline{v}_l|}{|\underline{v}_l| + |\underline{v}_m|} T_b$$

$$T_{am} = \frac{|\underline{v}_m|}{|\underline{v}_l| + |\underline{v}_m|} T_a$$

$$T_{bm} = \frac{|\underline{v}_m|}{|\underline{v}_l| + |\underline{v}_m|} T_b$$

$$T_0 = T_s - T_{al} - T_{am} - T_{bl} - T_{bm}$$

All the symbols have its usual meaning. Switching pattern for multilevel operation using large and medium vector is displays in Table 2.

## 5. SIMULATION RESULTS & DISCUSSION

Figure 5 shows the Matlab/Simulink model for the dual five-phase voltage source inverter for multilevel output in which the first block shows the generation of reference voltage. Magnitude and angle are the output of this block. This provides the switching signal for different semiconductors of voltage source inverter block devices with the help of Matlab code, repeating sequence signal, and zero-order hold circuit. The output of this block is stored in five-phase voltages in the voltage acquisition block workspace after passing through the low-pass filter block.

Figures 6(a) and 6(b) are showing the output phase voltages for INV 1 and INV 2 using only large vectors. Figure 7 displays filtered phase voltages of INV-1. The output voltages possess sufficient amount of third order harmonic along with small amount of 7th order harmonic. These harmonics are generated due to x-y components of space voltage vectors and will present in output whatever the reference voltage value may be when only large vectors are utilized to control the output of inverter. Figure 8 shows the filtered line voltages for INV 2.

Phase-to-Neutral value of Voltage Space Vectors for large vector and for medium vector is given by Eq. (6) and (7) respectively.

$$|\underline{v}_1| = 2/5V_{DC}\, 2\cos(\pi/5)\exp(jk\pi/5) \quad \text{for } k = 0,1,\cdots 9 \tag{6}$$

$$|\underline{v}_m| = 2/5V_{DC}\exp(jk\pi/5) \quad \text{for } k = 0,1,2\cdots 9 \tag{7}$$

Adjacent Line-to-Line value of Voltage Space Vectors for large vector and for medium vector is given by Eq. (8) and (9) respectively.

$$|\underline{V}_1| = \sqrt{1.382}\,* \; 2/5V_{DC}\, 2\cos(\pi/5)\exp(j(2k+1)\pi/10) \quad \text{for } k = 1,2\cdots 9 \tag{8}$$

$$|\underline{V}_m| = \sqrt{0.528}\,* \; 2/5V_{DC}\, 2\cos(\pi/5)\exp(j(2k+1)\pi/10) \quad \text{for } k = 1,2\cdots 9 \tag{9}$$

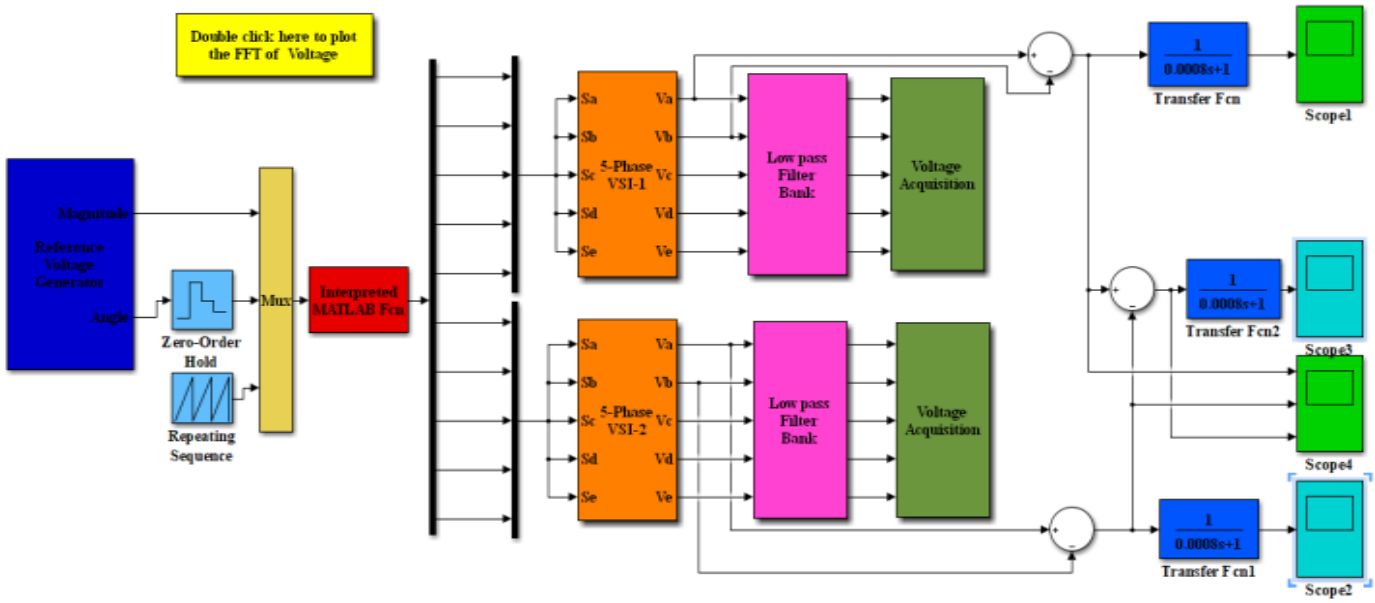


**Figure 5.** Matlab/Simulink Model of dual five-phase VSI

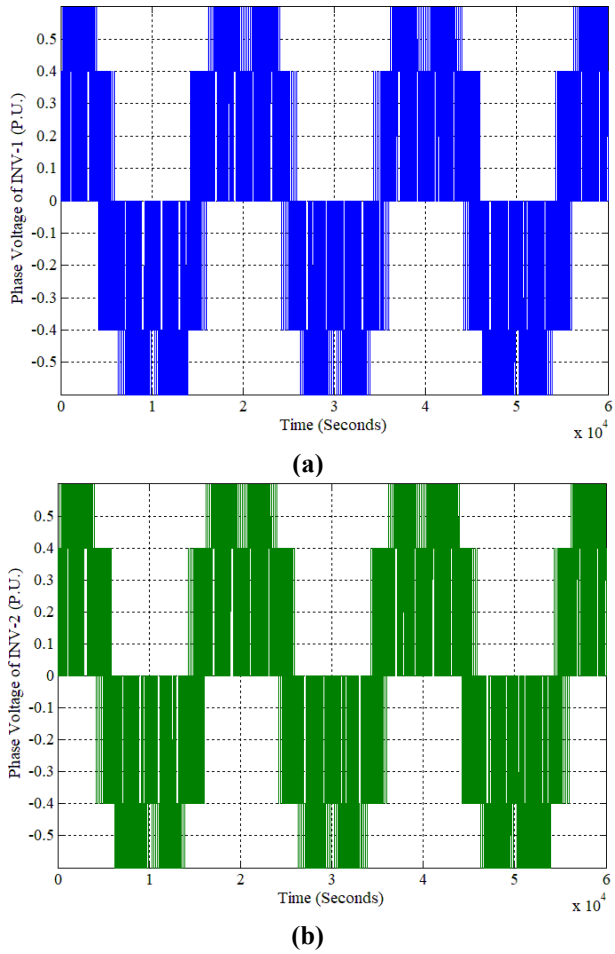


**Figure 6 (a).** Phase voltage of INV-1; **(b).** Phase voltage of INV-2

The dc-link voltage parameter is kept unity whereas switching frequency and fundamental frequency are 2 kHz and 50 Hz for simulation. Figure 9 shows the harmonic output spectrum for the voltage 'a' phase. It only has a fundamental voltage with a magnitude of 0.4218 p.u. r.m.s at a frequency of 50 Hz. The total harmonic distortion (THD) in the output is 23.97% and weighted total harmonic distortion (WTHD) is 12.46% of the fundamental, which shows that the results near the sinusoidal.

Simulation results for three-level operation using large and medium voltage vectors are in Figure 10 to Figure 12. Figures 10(a) and 10(b) display the phase voltages for INV-1 and INV-2 and Figure 11 show the filtered phase voltages for INV1. While Figure 12 shows the filtered line voltage for INV 2. All the parameters for simulation are kept the same.

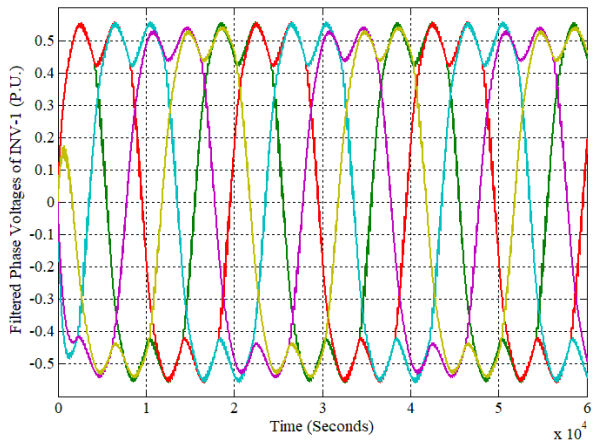


**Figure 7.** Filtered phase voltage of INV-1

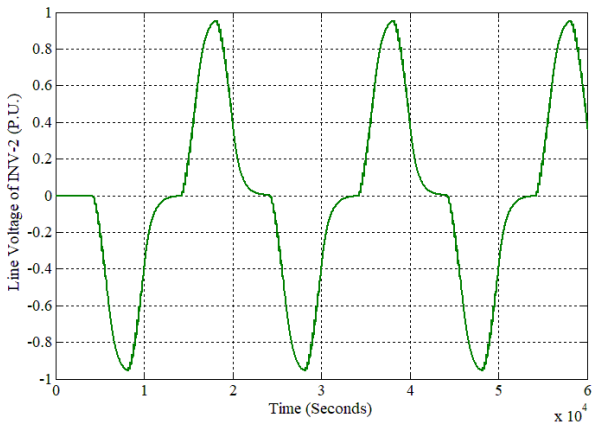


**Figure 8.** Filtered line voltage of INV-2

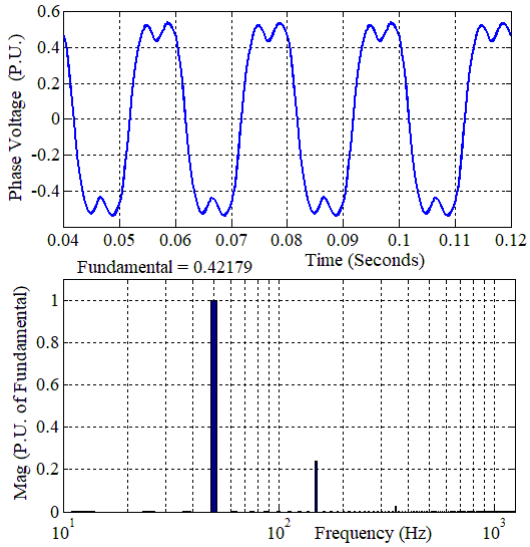


**Figure 9.** Harmonic spectrum of inverter output phase voltage

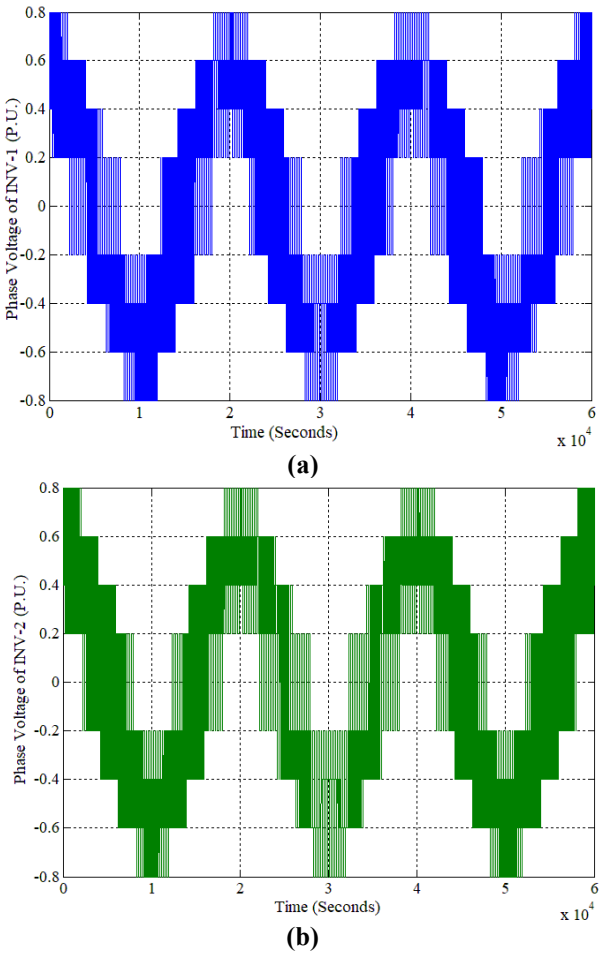


**Figure 10. (a).** Phase voltage of INV-1; **(b).** Phase voltage of INV-2

Figure 13 exhibits the harmonic spectrum of output for phase 'a' voltage. It contains only fundamental voltage having magnitude of 0.3756 p.u. r.m.s at a frequency of 50 Hz. The total harmonic distortion (THD) in the output is 3.30% and weighted total harmonic distortion (WTHD) is 1.81% of the fundamental, which is very less as compared to the previous scheme.

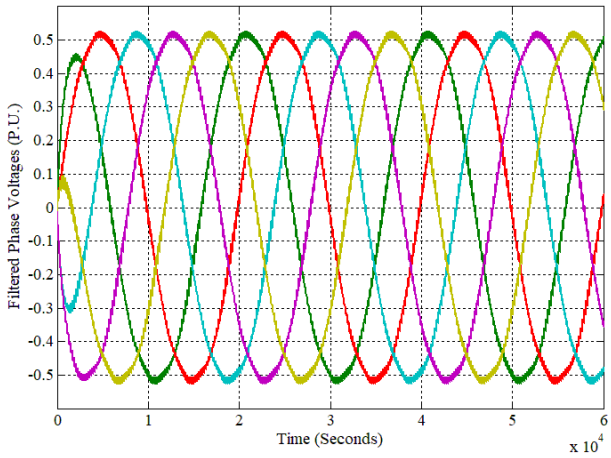


**Figure 11.** Filtered phase voltage of INV-1

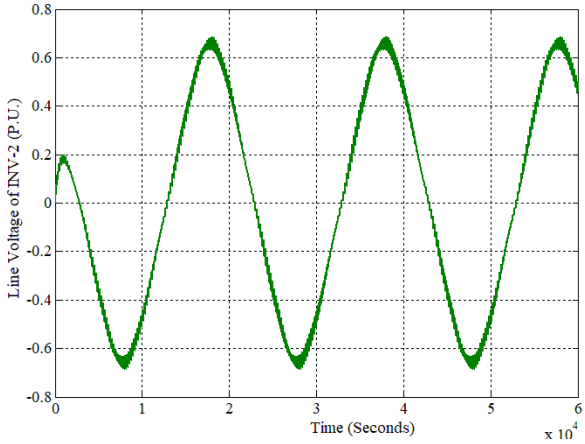


**Figure 12.** Filtered line voltage of INV-2

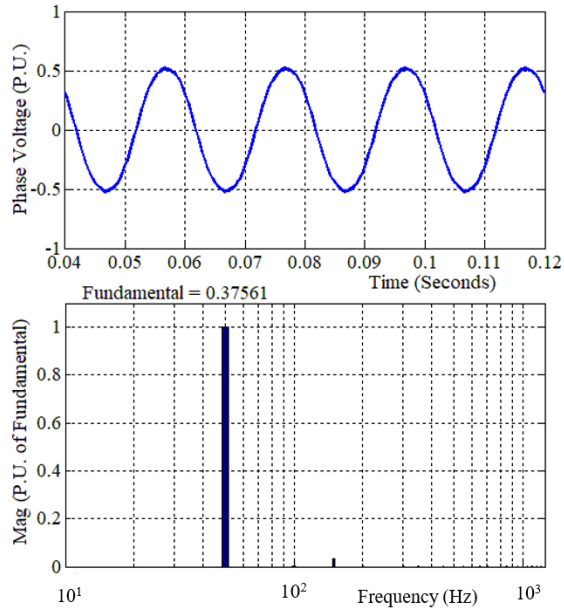


**Figure 13.** Harmonic spectrum of inverter output phase voltage

## 6. COMPARATIVE STUDY OF TWO SCHEMES

In accordance with the fundamental Component, THD, and WTHD, the contribution of both the presented SVPWM

scheme has been examined and a comparative analysis has been concluded. The comparison of both SVPWM schemes is shown in Table 3 and Figure 14 is showing the bar chart for quick comprehension. It is clear here that, compared to the first SVPWM scheme, the scheme using large and medium voltage vectors has very low order harmonic content.

The time of application of large and medium vectors is proportionally divided according to their length. The first system offers sinusoidal efficiency, but only up to 85.41% of the total achievable basic output is operational. The second scheme makes it possible to fully utilise the available DC bus voltage. It is known that the highest reference value to be reached is between 85.41% and 100%. The inverter's reference voltage exceeds the maximum output circle because of this. The application time of different voltage vectors is dependent on the voltage and variable amplitude of the reference voltage.

The study shows that using only large vectors to validate the concept, the output contains 23.97% THD and 12.46% WTHD, which indicates that the losses are substantial. It is because the output contains a sufficient amount of 3rd order harmonics i.e. 23.8349% and a small amount of 7th order harmonics i.e. 2.504650%.

When the author uses the large and medium vectors together, the results are much better compared to the previous scheme to reduce THD. The output includes 3.30% THD and 1.81% WTHD only using large and medium vectors. 3rd order harmonics decrease from 23.834% to 3.2474% and 7th order harmonic has reduced to 2.50% to 0.436947%

**Table 3.** Comparison of both the SVPWM Schemes

| Description | using large vector only | using large & medium vectors |
|---|---|---|
| Fundamental Component | 42.18% | 37.56% |
| Total Harmonic Distortion | 23.97% | 3.30% |
| Weighted Total Harmonic Distortion | 12.46% | 1.81% |
| 3rd order Harmonic | 23.834900% | 3.247490% |
| 7th order Harmonic | 2.504650% | 0.436947% |

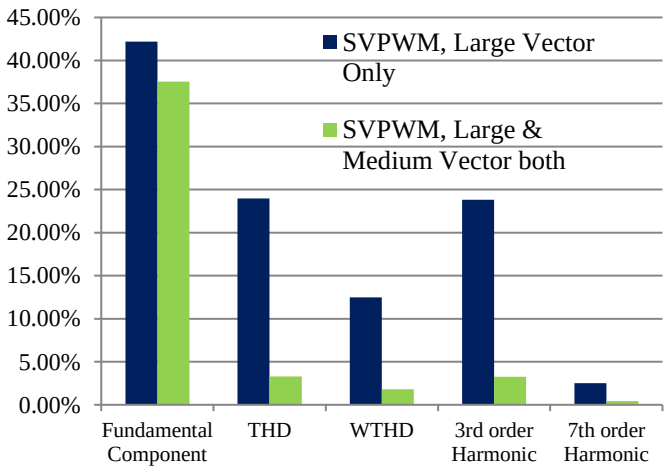


**Figure 14.** Bar chart of both SVPWM scheme

## 7. CONCLUSION

In this paper, two SVPWM schemes for a two-level five-phase dual voltage source inverter are presented to achieve multilevel performance. The first scheme is by using large vectors only, which generates the non-sinusoidal output results due to significant low-order harmonics presence. Another approach utilizes both large and medium voltage vectors to obtain sinusoidal output results, which shows that as compared to the first scheme, the second technique has low values of low-order harmonics. These SVPWM techniques are easy and effective to implement. The presented schemes may apply easily in high power medium voltage applications. A similar concept may be extended to a higher phase number inverter system in the future along with a practical realization.

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## NOMENCLATURE

| | |
|---|---|
| SVPWM | Space Vector pulse width modulation |
| VSI | Voltage source inverter |
| THD | Total harmonic distortion |
| WTHD | Weighted total harmonic distortion |
| NPC | Neutral point clamped |