A novel control method for five-level H-bridge/neutral point clamped inverter

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ABSTRACT. *Considering the complexity in the calculation of reference vectors and the selection of switching states, this paper puts forward a novel algorithm for the space vector pulse width modulation (SVPWM) for multi-level inverters. By this algorithm, the multi-level SVPWM is generated by triangulating the sector to a two-level sector in space vector diagram and using the two-level SVPWM formulas, thereby eliminating the need for lookup tables in sector identification. The proposed algorithm can be extended to an n-level inverter, which is easy to achieve and suitable for high-power, high-voltage applications. Then, an H-bridge/neutral point clamped (H-NPC) inverter was adopted to explain the proposed algorithm. Finally, the proposed algorithm was proved valid through simulation experiments.*

RÉSUMÉ. *Compte tenu de la complexité du calcul des vecteurs de référence et de la sélection des états de commutation, cet article propose un nouvel algorithme pour la modulation de largeur d'impulsion du vecteur spatial (SVPWM) pour les onduleurs à multi-niveaux. Grâce à cet algorithme, le SVPWM multi-niveaux est généré en triangulant le secteur à un secteur à deux niveaux dans le diagramme vectoriel spatial. En utilisant les formules SVPWM à deux niveaux, on élimine ainsi le besoin de tables de recherche dans l'identification sectorielle. L'algorithme proposé peut être étendu à un onduleur de niveau n, qui est facile à réaliser et convenable pour les applications à haute puissance et à haute tension. Ensuite, on adopte un onduleur H-Bridge/point neutre (H-NPC) pour expliquer cet algorithme proposé. Enfin, l'algorithme proposé a été prouvé valide par des expériences de simulation. Enfin, la validité de cet algorithme proposé a été confirmée par des expériences de simulation.*

KEYWORDS: *multi-level, triangulation, space vector pulse width modulation (SVPWM), H-bridge/neutral point clamped (H-NPC) inverter.*

MOTS-CLÉS: *multi-niveaux, triangulation, modulation de largeur d'impulsion du vecteur spatial (SVPWM), onduleur H-Bridge/point neutre (H-NPC).*

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1. Introduction

Multilevel inverters are widely applied to fields of medium-voltage high-power transmission (Kouro *et al*., 2010; Wiechmann *et al*., 2008; Harnefors *et al*., 2013). PWM is used to control multilevel inverters to generate discrete VVVF, where two of the main strategies for PWM are SPWM and SVPWM (Celanovic and Boroyevich, 2001; Yao *et al*., 2008; Mcgrath *et al*., 2003; Kouro and Rebolledo, 2007; Gupta and Khambadkone, 2006; Gupta and Khambadkone, 2007; Gupta and Khambadkone, 2007; Gopinath *et al*., 2009). For multilevel SPWM, the comparison of reference signals and carrier signals generates PWM; while in terms of SVPWM, three nearest voltage vectors around the reference vector are used to synthesize the reference vector (Van Der Broeck *et al*., 1988). SVPWM has the advantages of better fundamental wave output, better harmonic performance and easy implementation with digital signal processor. It can be achieved through the following steps: 1) identify locations of the reference vector; 2) determine three nearest synthesizing vectors around the reference vector; 3) calculate the on-time for each synthesizing vector; 4) choose optimized switching sequences.

To identify sectors, coordinates of the reference vector can be transformed to two dimensional coordinates. Another method is to decompose the reference vector to three-phase coordinate systems and to compare it with three-phase discrete phase voltage. After sectors are identified, the voltage vector of the sector tip can be identified. The synthesizing voltage vector of the sector tip and the switching sequences can be obtained from lookup tables. Calculation of on-time can help map the identified sector into the corresponding sector in the two-level vector diagram (Cheng and Wu, 2007; Aneesh Mohamed *et al*., 2009).

In order to achieve high output voltage in high-power transmission, a cascade inverter structure with clamped multi-level inverters and power units in series is usually adopted (Buccella *et al*., 2014; Yao *et al*., 2008; Zhang *et al*., 2011). How to calculate switching state and vector action time simply and effectively has always been a hot topic in the research of multilevel inverters.

In the paper, a novel SVPWM algorithm is studied. In the n-level voltage vector diagram, each sector can be divided into four subsectors, and each subsector can be further separated into four smaller sectors until an equivalent two-level sector is formed. The sector that contains reference vectors is mapped into the two-level sector, whose two-level SVPWM is used to generate multilevel SVPWM. The proposed algorithm uses simple equations to identify sectors, thus there is no need to refer to lookup tables. Redundant vectors as needed can be obtained automatically without lookup tables. The proposed algorithm for generating SVPWM for multilevel inverters is explained for a five-level HNPC inverter. The generalized algorithm can be extended to any n-level inverter.

2. Five-level HNPC inverter topology

Phase A of the five-level HNPC inverter is composed of two NPC bridge arms.

Its topology is shown in Figure 1, where S_{a11}, S_{a12}, S_{a13}, S_{a14}, S_{a21}, S_{a22}, S_{a23}, S_{a24} are power electronic switching devices. Each bridge arm has two clamped diodes. The DC side voltage is 2E, the capacitance C_{a1}=C_{a2}, and all of the capacitor voltages are E. Phase B and phase C share the same structure with phase A. Table 1 shows the relationship between the output voltage of the five-level HNPC inverter (u_{an}) and switching states, where "1" denotes the turn-on state of the switching devices and "0" denotes the turn-off state of the switching devices.

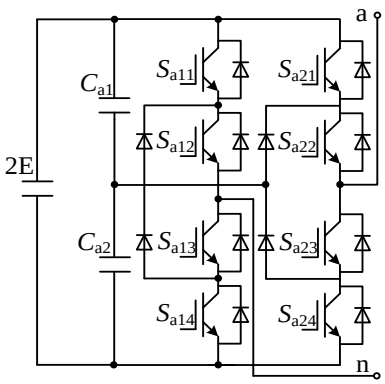

Figure 1. Five-level HNPC inverter topology of phase A

Table 1. Relationship between u_{an} and switching states

u_{an}	S_{a11}	S_{a12}	S_{a13}	S_{a13}	S_{a21}	S_{a22}	S_{a23}	S_{a24}
-2E	1	1	0	0	0	0	1	1
-E	0	1	1	0	0	0	1	1
0	0	1	1	0	0	1	1	0
E	0	0	1	1	0	1	1	0
2E	0	0	1	1	1	1	0	0

3. Five-level voltage vector diagram triangularization

Figure 2 shows the space vector diagram for a five-level inverter in sector I. The three vectors, namely A_{00}, A_{01} and A_{02}, constitute sector I of the two-level vector diagram. The three voltage vectors, namely A_{11}, A_{12} and A_{13}, locate at each neutral point of the sector boundaries, respectively. The above six vectors divide sector I($\Delta A_{00}A_{01}A_{02}$) into four small sectors, forming a three-level sector. In addition, there are nine other vectors that locate at A_{21}, A_{22}, A_{23}, A_{24}, A_{25}, A_{26}, A_{27}, A_{28} and A_{29}, respectively. They locate at each neutral point of the three-level sector boundaries,

respectively. All of the above 15 vectors divide sector I of the five-level voltage vector diagram into 16 small sectors. Therefore, if each large sector of a n-level vector diagram is regarded as a two-level sector, which is divided into four smaller sectors, it will form a three-level voltage vector diagram. And if each sector of the three-level voltage vector diagram is further divided into four smaller sectors, a five-level voltage vector diagram is then formed. Such pattern continues until a n-level voltage vector diagram is formed.

The voltage vector diagram of a three-phase voltage source inverter is regular hexagon with six sectors. As the six sectors share the same structure, the proposed algorithm is explained only for the first sector, being explained in the same way as the other five sectors.

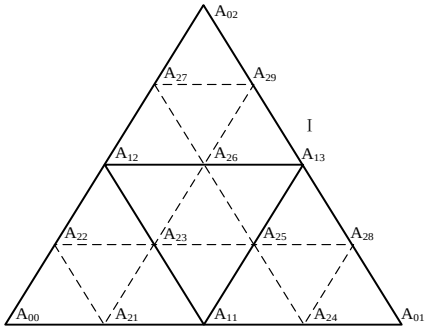

Figure 2. Space vector diagram for a five-level inverter in sector I

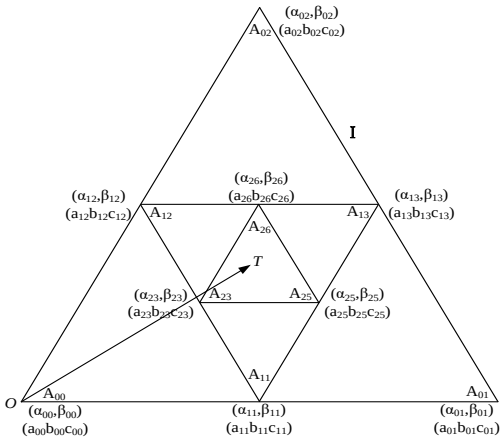

Figure 3. Sector identification and switching vector determination

Triangularization of the voltage vector diagram means a constant division of a multilevel voltage vector diagram into small sectors. For each stage, referring to the neutral point of the sector boundary, each sector is divided into four small sectors. Such pattern continues until a higher level voltage vector diagram is formed. For instance, as shown in Figure 3, in two-level sector Ⅰ, the coordinates of the three vectors A_{00}, A_{01} and A_{02} are (α_{00}, β_{00}), (α_{01}, β_{01}) and (α_{02}, β_{02}), respectively. The coordinates of A_{11}, A_{12} and A_{13} that are located at the neutral points of the sector boundaries can be obtained from those of A_{00}, A_{01} and A_{02}. For example, the coordinate of A_{11} is obtained by equation (1) as follows.

$$\begin{aligned} \alpha_{11} &= \frac{1}{2}(\alpha_{00} + \alpha_{01}) \\ \beta_{11} &= \frac{1}{2}(\beta_{00} + \beta_{01}) \end{aligned} \tag{1}$$

The coordinates of A_{12} and A_{13} can be obtained in a similar way. The switching states of A_{00}, A_{01} and A_{02} are ($a_{00}b_{00}c_{00}$), ($a_{01}b_{01}c_{01}$) and ($a_{02}b_{02}c_{02}$), respectively. The switching vectors A_{11}, A_{12} and A_{13} are represented by ($a_{11}b_{11}c_{11}$),($a_{12}b_{12}c_{12}$) and ($a_{13}b_{13}c_{13}$), respectively. Taken A_{11} as an example, its switching state is given as:

$$x_{11} = \frac{1}{2}(x_{00} + x_{01}) \tag{2}$$

where x denotes the three phases, namely a, b and c. Equation (1) and equation (2) are used to generate voltage vectors that locate at the neutral points of the sector boundaries to further divide the triangular sector into four small sectors.

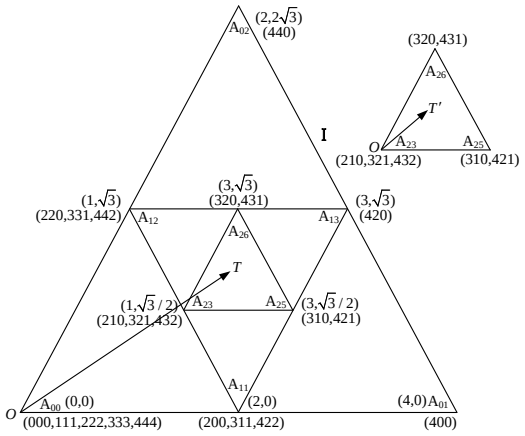

Figure 4. Mapping of a reference space vector OT

Sector 1 is taken as an example to explain the proposed algorithm in the paper. The coordinates of the three sectors in sector 1, namely A_{00}, A_{01} and A_{02}, are (0,0), (4,0) and (2,2√3), respectively. A_{00}, the zero vector, contains five redundant vectors, namely (000), (111), (222), (333) and (444). There is only one switching state for A_{01} and A_{02}, namely (400) and (44), respectively. With equation (1), it is calculated that the coordinate of A_{11} is (2,0). With equation (2), it is calculated that the switching state of A_{11} is (200), (311) and (422). In a similar way, the coordinates and switching states of A_{12} and A_{13} can be obtained.

4. Five-level SVPWM algorithm

The proposed algorithm for generating SVPWM for multilevel inverters is explained for a five-level HNPC inverter. SVPWM is achieved through the following four steps: 1) sector identification; 2) determination of synthesizing vectors; 3) calculation of the on-time for each synthesizing vector; 4) optimization of switching sequences.

4.1. Sector identification and switching vector determination

Through repeated usage of the triangularization equations, the sector of the reference vector is identified. The three vertices of smaller sectors denotes the voltage vectors of the synthesizing reference vector. The three-phase instant voltage value (u_a, u_b, u_c) is used to identify the coordinate (α,β) of the reference vector. The coordinate of n-level vector should be divided by V_{dc}/(n-1) to generate the corresponding per-unit coordinate, where V_{dc} denotes DC side voltage. In the five-level vector diagram, the six vectors that form the periphery of the regular hexagon are the same with those of the two-level regular hexagon.

As shown in figure 4, the reference space vector OT is used to explain five-level triangularization. Firstly, we identify the location of the large sector that contains the reference vector. The reference vector is composed of A_{00}, A_{01} and A_{02}. The coordinates of its vertices are (0,0), (4,0) and (2, 2√3), respectively, and its corresponding switching states are shown in Figure 4. The redundant state that exists in the switching states of A_{00} is (000,111,222,333,444). The switching states of A_{01} and A_{02} are (400) and (440), respectively. The five-level vector diagram demands two calculations. For the first one, there come four small triangles. The newly generated vectors locate at A_{11}, A_{12} and A_{13}, which divide sector 1 into four small sectors, namely $\Delta A_{00}A_{12}A_{11}$, $\Delta A_{11}A_{12}A_{13}$, $\Delta A_{11}A_{13}A_{01}$ and $\Delta A_{12}A_{02}A_{13}$.

The average coordinate value of the three vertices of the small hexagon is the centroid. For the equilateral triangle, the coordinates of its vertices are (α_1,β_1),(α_2,β_2) and (α_3,β_3), respectively. The equation of the centroid $(\alpha_{cent},\beta_{cent})$ is given as:

$$\alpha_{\text{cent}} = \frac{1}{3}(\alpha_1 + \alpha_2 + \alpha_3)$$
$$\beta_{\text{cent}} = \frac{1}{3}(\beta_1 + \beta_2 + \beta_3) \tag{3}$$

The small sector whose reference vector is the nearest to the centroid is $\Delta A_{11}A_{12}A_{13}$. For the five-level vector diagram, another triangularization calculation is done to divide $\Delta A_{11}A_{12}A_{13}$ further into four smaller sectors, thus identifying that the reference vector is located at $\Delta A_{23}A_{26}A_{25}$. Once the sector is identified, one can obtain the corresponding synthesizing vector of the sector vertex.

4.2. Calculation of the on-time of the synthesizing vector

The second step is to calculate the on-time of the synthesizing vector, where the multilevel reference vector can be mapped into a two-level reference vector. A virtual zero vector in the sector is used to map the reference sector into the two-level sector. The virtual zero vector is defined as the vector with the minimum sum of the absolute coordinate values of (α,β), representing the deviation degree from a real zero vector. Thus, we choose a virtual vector that has the minimum deviation from the zero vector.

As shown in Figure 4, in sector identification, *OT* is located at $\Delta A_{23}A_{26}A_{25}$. The coordinates of the vectors A_{23}, A_{26} and A_{25} are (0,0), (4,0) and (2, 2√3), respectively. The sum of the absolute coordinate values of A_{23} is minimum, thus A_{23} is chosen as the virtual zero vector to map the multilevel reference vector *OT* into a two-level reference vector *OT'*. After the mapping, equations in Table 2 can be used to obtain T1 and T2, the on-time of two nonzero vectors. And we can further determine T_0, the on-time of the virtual zero vector.

Table 2. Equations for determining T_1 and T_2 for a two-level inverter

sector	T_1	T_2
I	$T_s[v_\alpha - v_\beta / \sqrt{3}]$	$T_s[v_\beta / 0.866]$
II	$T_s[v_\alpha + v_\beta / \sqrt{3}]$	$T_s[-v_\alpha + v_\beta / \sqrt{3}]$
III	$T_s[v_\beta / 0.866]$	$-T_s[v_\alpha + v_\beta / \sqrt{3}]$
IV	$T_s[-v_\alpha + v_\beta / \sqrt{3}]$	$-T_s[v_\beta / 0.866]$
V	$-T_s[v_\alpha + v_\beta / \sqrt{3}]$	$T_s[v_\alpha - v_\beta / \sqrt{3}]$
VI	$-T_s[v_\beta / 0.866]$	$T_s[v_\alpha + v_\beta / \sqrt{3}]$

4.3. Optimization of switching sequences

Once the synthesizing vector and on-time are determined, it is required to optimize switching sequences so that there is the change of only one switching state per time. For each switching period, redundant vectors of the virtual zero vector are used to optimize switching sequences. We take *OT* in Figure 4 as an example. Its vertex is located at $\Delta A_{23}A_{26}A_{25}$, where A_{23} is the virtual zero vector. The corresponding switching states of the sector are A_{23}(210,321,432), A_{26}(320,431) and A_{25}(310,421). There are three redundant switching states for the virtual zero vector and two for the voltage vectors A_{25} and A_{26}. In the paper, the following strategy is used to treat redundance: if there are over two redundant degree for the virtual zero vector, all can be chosen except for the last redundant vector. The reason is that the switching sequences will fail to be optimized if the last one is chosen. The switching state of the virtual zero vector is used alternately during the first switching period. During one switching period, the optimized switching sequences are (321)→(421)→(431)→(432)→(431)→(421)→(321). Therefore, optimized switching sequences can be obtained by a proper selection of the redundant switching states of the virtual zero vector without lookup tables.

5. Analysis of simulative results and experimental results

To verify the validity of the method in this paper, we establish a five-level HNPC inverter prototype and adopt the controller with DSP and FPGA, which is shown in Figure 1. DSP uses TI's TMS28335 to complete the main program and SVPWM operations. FPGA uses Actel's A3P250 and is responsible for the driving signals of the switch devices with the sampling frequency fs = 2kHz and the modulation degree m_i=0.9. Prototype parameters are: the DC side capacitance C=4700μF, the capacitor voltage E=100V, and the three-phase symmetric resistance-inductance load L=3mH, R=10Ω. Figure 5 shows the phase voltage u_{an} and line voltage u_{ab} simulative waveforms. Figure 6 shows the line voltage u_{ab} and phase current i_a experimental waveforms. The simulative waveforms and experimental waveforms have good quality and is capable of verifying the validity of the proposed algorithm.

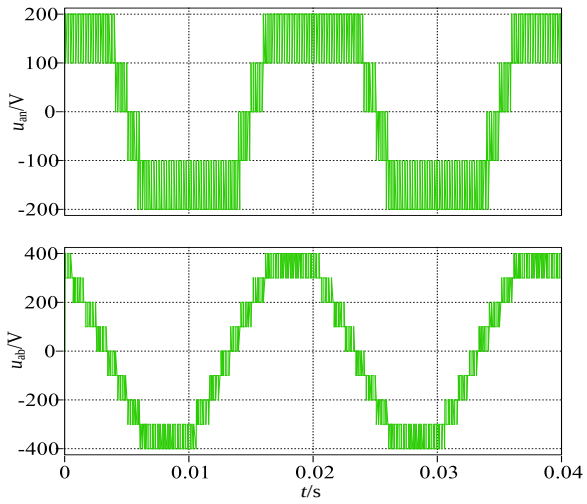

Figure 5. Phase voltage and line voltage waveform, m_i=0.9

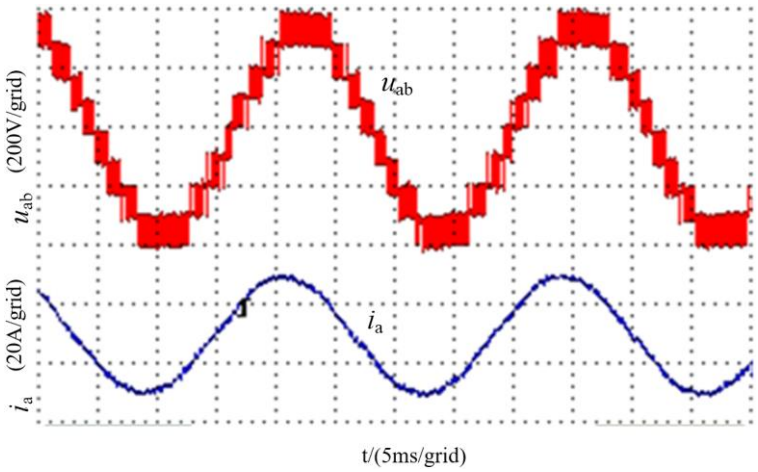

Figure 6. Line voltage and phase current waveform, m_i=0.9

6. Conclusion

This paper researches a general space vector pulse width modulation (SVPWM) for multilevel inverters. This easy and effective algorithm takes advantage of sector triangularization in identifying positions of reference vectors. After sector identification is finished, the switching states of corresponding switching vectors

can be generated simultaneously without lookup tables. The two-level SVPWM formulas is used to generate multilevel SVPWM. The proposed method for generating SVPWM for multilevel inverters is validated for a five-level HNPC inverter, and simulative and experimental results verify the validity of the method in this paper.

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