Dynamic IGBT model

Application to top-metal ageing effects on chip electro-thermal distributions during short circuit operations

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ABSTRACT. *An innovative model of IGBT has been carried-out to monitor temperature distributions and current sharing with in an IGBT chip during critical operations. The aim of this paper is to highlight the electro-thermal stress and their effects on the semiconductor IGBT chip and its immediate vicinity, by evaluating the effects of damage using distributed models. One of the failure mechanisms in IGBT (Latch-up) is due to the "switch on" of the NPNP parasitic thyristor. This IGBT damage mechanism leads in many cases to the destruction of the component. In this paper dynamic latch-up failures during IGBT short-circuit operations has been performed*

RÉSUMÉ. *Un modèle électrothermique distribué d'une puce IGBT a été développé afin de mettre en évidence par simulation un phénomène de latchup dynamique observé expérimentalement lors de la coupure d'un courant de court-circuit sur ces composants. Ce modèle est basé sur un couplage d'un réseau thermique de Cauer 3D et d'un réseau de macro-cellules IGBT, chacune sur la base du modèle électro-thermique IGBT d'Hefner, représentant la puce discrétisée spatialement. Le modèle Hefner a été modifié pour pouvoir prendre en compte l'effet du* latchup. *Le couplage est direct et fonctionne sous l'environnement Simplorer en VHDL-AMS. Le modèle a été utilisé pour rendre compte de l'impact du vieillissement de la métallisation de la puce sur la redistribution des températures et des courants entre macro-cellules lors du phénomène de court-circuit. Il a également été utilisé pour montrer l'influence éventuelle de ce même vieillissement sur le phénomène de* latchup *dynamique.*

KEYWORDS: *electro thermal modeling, IGBT, short-circuit, reliability, ageing, dynamic latch-up.*

MOTS-CLÉS : *modèle électrothermique, IGBT, court-circuit, vieillissement de la métallisation,* latch-up *dynamique.*

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1. Introduction

Power modules, organized around power chips (IGBT, MOSFET, Diodes ...), are increasingly needed for transportation systems such as rail, aeronautics and automobile. In all these applications, power devices reliability is still a critical point. This is particularly the case in the powertrain of hybrid or electric vehicle in which power chips are often subjected to very high electrical and thermal stress levels which may affect their reliability. Thus, the ability to analyze the coupled phenomena and to accurately predict degradation mechanisms in power semiconductors and their effects due to electro-thermal and thermo-mechanical stress is essential. Especially on the semiconductor chip where significant physical interactions occur and its immediate vicinity. This is especially the case for critical operations such as pulsed over-currents, short-circuits and avalanche regimes where these distributions are both highly distributed inside the semiconductor devices. This is not only due to the electro-thermal coupling but also to the spatial bond-wire contact configuration on the top metal. Until now, experimental measurements allow to provide only spatial distributions of temperature in such electrical regimes. This can be done by high-speed infrared thermography for example. Nevertheless, great difficulties occur when trying to characterize the current distributions over the surface of the chip. So, only numerical models can predict electro-thermal coupling between elementary cells of a power device on such critical and brief electrical regimes. Among these models, we can typically find physical models based on the finite element method and only focused on one cell (Pendharkar et al, 1998; Benmansour et al, 2007). Other physical models implemented in circuit software environments, such as Simplorer or Pspice (Hefner, 1994; Dia *et al.,* 2009), can be used to simulate several paralleled cells in order to represent the electro-thermal interaction, inside a same chip, between a large number of elementary cells (Irace *et al.,* 2007; Codecasa *et al.,* 2003; Riccio *et al.,* 2010). Nevertheless, the electrical representation used for such models must remain sufficiently light for the trade-off between computing time and complexity.

The modeling strategy consists on a discretization of the power semiconductor chip in macro-cells with a distributed electro-thermal behavior over the chip area. In case of the IGBT devices, each macro-cell is governed by the Hefner model (Hefner, 1994) and electrically linked by their terminals. Temperature variations used in these macro-cells are obtained by a nodal 3D-RC thermal model. This allows the distributed electro-thermal problem to be solved homogeneously and simultaneously by a circuit solver such as SIMPLORER.

The aim of this model is to allow the accurate analysis of some effects in the electrical and thermal coupling over the chip. Above all, this model should explain some effects such as the contacts position over the emitter area and the ageing of the chip emitter metallization. So, the electric models for the elementary cells must be of a sufficiently high level. For computation time reasons, the number of elementary cells must be limited. In a first step, the model is used to clarify how the current and

the temperature map are distributed over the chip according to the relative positions between cells and wire bond contacts on the top-metal during short-circuit operation. In a second step, we will show how dynamic latch-up failures may occur during short-circuit process.

2. Modelling strategy

The modeling strategy consists on a discretization of the power semiconductor chip in macro-cells with a distributed electro-thermal behavior over the chip area. By discretizing the chip into multiple box-shaped volumes, we can define an equivalent macro-cell resulting from all elementary cells in each of these volumes.

2.1. Thermal component

In order to compute the local temperature of each IGBT macro-cell, a thermal model of the power module assembly has been carried out. In this example (Figure 1), the assembly is composed by different material layers (chip, die-attach, substrate).

The chosen modeling strategy is a nodal method with a 3D-RC Cauer network. Material layers are discretized in volume elements which are characterized by a thermal capacitance and thermal resistances in the three space directions. Thermal sources are added for the IGBT volume elements which are inputs from the electrical component P_{ij}, (Figure 1). The temperature is computed in the central node of each volume element and is used as output for the electrical component.

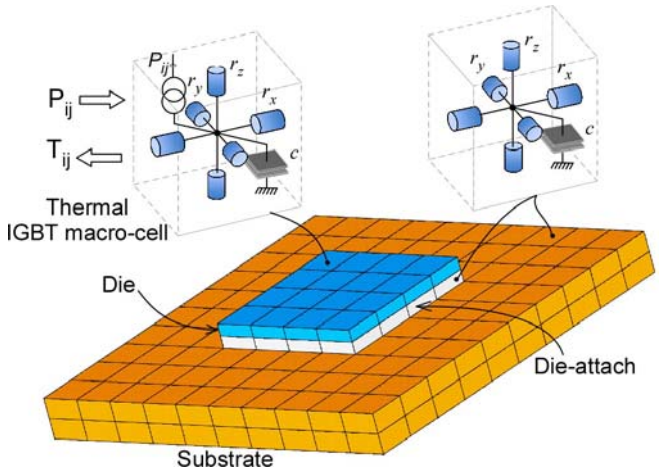


Figure 1. Thermal component

The 3D-RC thermal network is generated with an algorithm which takes into account geometry, thermal properties and boundary conditions. It is written in VHDL-AMS language in order to be compatible with the electrical component. The material dimensions and properties are given in Table 1.

The 3D-RC model finally includes a silicon layer corresponding to the silicon chip and a SnAg solder layer. The third layer is the Cu substrate. Thus, for a discretization level of (4×4), chip and solder present the same number of cells of 250 um x 250 um x 25 um (*i.e.* 16 cells and 25 nodes). While the substrate present in this case 64 volume elements 250 microns x 250 microns x 25 microns, *i.e.* 65 nodes. The 3D-RC model with mesh of 4×4 present a total of 96 cells and 115 nodes.

Table 1. Materials and properties

Layers	Die	Die-attach	Substrate
Materials	Silicon	SnAg	Copper
Dimensions (cm×cm×µm)	1×1×100	1×1×100	4×4×2000
Thermal conductivity (W/m.K)	150	53	400
Specific heat (J/kg K)	703	213	385
Density	2340	7280	8960

2.2. Electrical component

Each IGBT macro-cell in Figure 2, is an IGBT model derived from the Hefner model (Hefner, 1994) where electrical parameters are temperature dependent. The emitter terminals of these macro-cells are connected to each other by a resistance grid representing the chip emitter metallization (Figure 2). As well, gate terminals are connected by a poly-silicon gate resistance grid and collector terminals are directly connected to each other.

The resistance network of the emitter metal layer has been identified by a finite element model of an equivalent aluminum layer of 3 µm thickness. Finally, each IGBT macro-cell model is implemented in VHDL and provides the local electrical power dissipation of the corresponding thermal cell of the thermal model. In turn, it requires, as input, the local temperature value computed by this last one (T_{ij} in Figure 2).

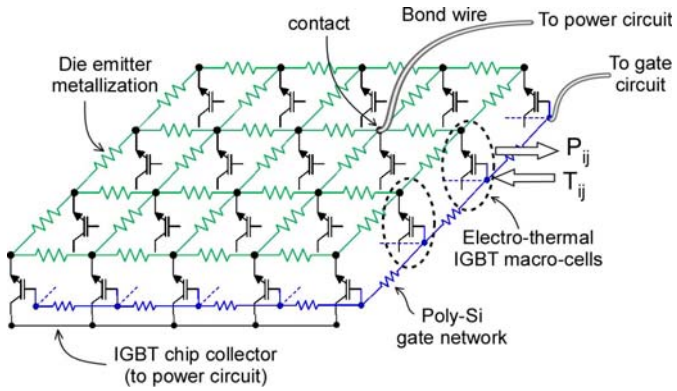


Figure 2. Electrical component

3. Inclusion of the latch-up

In order to take into account latch-up events, due to the parasitic npn transistor as shown in Figure 3a, the Hefner model has been modified by introducing an Ebers-Moll model in normal forward mode. For simplification reason only the threshold triggering of the latch-up has been modeled. This has been realized by a current source (I_{latch}) controlled by the voltage through the emitter to P-body resistance (R_{sh}) beyond a threshold voltage of 0.6V.

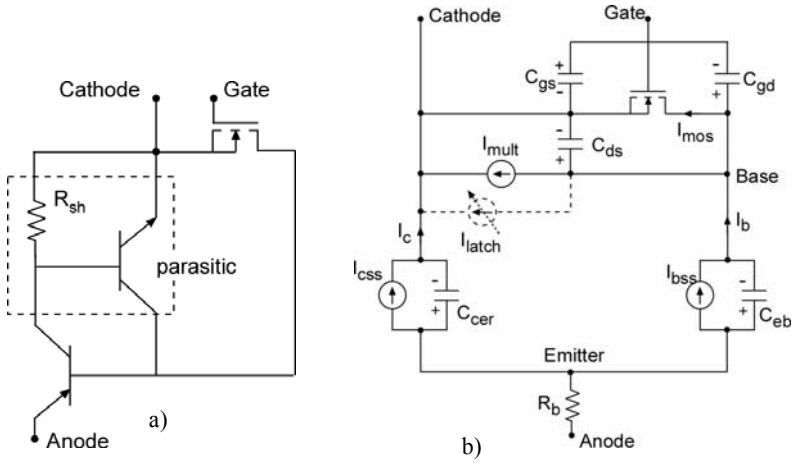


Figure 3. a) Parasitic npn transistor; b) Electrical model used for each IGBT macro-cell

The body resistance (R_{sh}) was estimated at about 6 mΩ for the whole chip with approximately 90 000 paralleled cells. As it will be said later, the die has been divided in 4×4 macro-cells for this study. So, the body resistance of a macro-cell is approximately 90 mΩ. The modified Hefner model used for each macro-cell is given in Figure 3b.

Finally, these two components are implemented in the Simplorer software and simultaneously solved.

4. Application to metallization ageing impacts

In this paper, the given simplified example is based on a verified VHDL IGBT model (Ibrahim *et al.,* 2007) with parameters corresponding to an IGBT which is rated at 30A-600V non-punch through (NPT) device. For experimental comparison and validation, one can refer to (Ibrahim *et al*., 2007).

The IGBT die has been divided in 4×4 box-shaped volumes and only one bonding wire with only one bond contact is taken into account. For these simulations, the power device has been assimilated to a multi-layer stack of materials and thermal conduction is considered in the three space dimensions. As boundary conditions, lateral and upper surfaces are considered as adiabatic and convective exchange is taken into account at the bottom surface of the substrate with a convective coefficient $h = 1000\ W.m^{-2}.K^{-1}$, reflecting the convective exchange with a liquid. The model has been used to highlight the electro-thermal behavior during short-circuit conditions. In this section, it has been used to clarify how the current and the temperature maps are distributed over the chip according to the relative position between cells and wire bond contacts on the top-metal. As shown in (Lefebvre *et al*., 2005; Pietranico *et al*., 2010; Arab *et al*., 2008), during repetitive short circuit operations, an ageing process takes place especially on the emitter metallization of the device.

As illustration, we will analyze the effects of this material degradation on the current sharing and temperature distribution between macro-cells. For this purpose, the schematic circuit of Figure 4a was used. The power circuit consists of a source voltage that was set to 450 V, parasitic elements, $R_p = 5$ mΩ and L_p=10 nH. Gate circuit is simplified with a gate resistance ($R_g = 2$ Ω) and gate voltage source (E_g).

The computed short-circuit waveform is given in Figure 4b. The collector voltage is linearly increased until 450V is reached, then at t = 20µs, the device is switched-on and short-circuit is operated during 30µs before the device is turned off. An over-voltage, due to the parasitic inductance Lp, is produced in the power circuit during the switch-off.

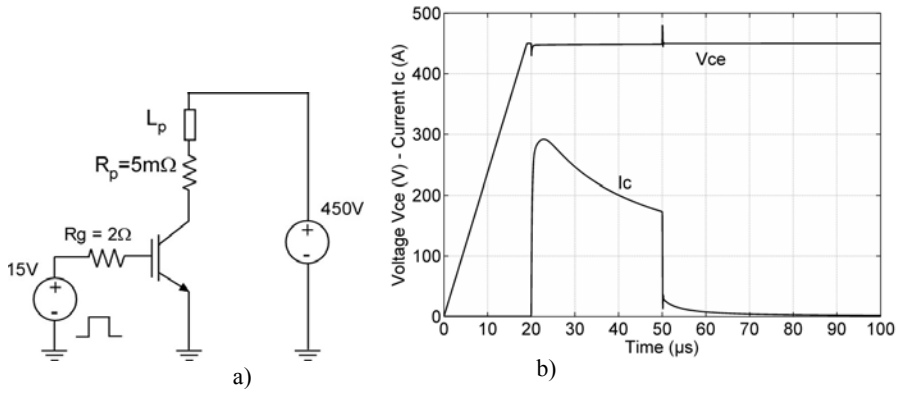


Figure 4. a) Electrical circuit; b) Simulated short-circuit operation (Lp=10nH)

4.1. Effect of aging on the waveforms of total short circuit

In order to highlight the top-metal ageing effects in this last characteristic, we show in the following what happens when this layer is more resistive. The emitter metallization corresponds to a 3 µm thick aluminum layer with a surface area equal to that of the IGBT chip. At initial state, before ageing, the electrical conductivity of this material is 38×106 S.m-1 (σ0).

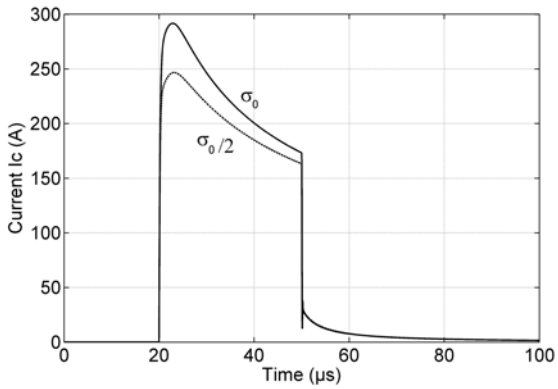


Figure 5. Top-metal ageing effect on the short-circuit current

Previous works have demonstrated that electrical conductivity of this layer can be reduced by a factor of more than 2 after ageing in repetitive short-circuit conditions (Pietranico *et al.*, 2010; Arab *et al.*, 2008). So, the simulation of the aged metallization is performed with an electrical conductivity of 19×106 S.m-1 (σ0/2). The resistance network of the chip top-metal, visible in Figure 1, has been obtained

by identification with a finite element model of this layer. As a result, we can see the decrease of short-circuit current level due to the aging of the metallization layer in Figure 5. Such a result has been already observed experimentally (Arab *et al.*, 2008).

4.2. Effect of aging on the current distributions

The total short-circuit current of the initial device is shared between the macro-cells as given in the upper graph of Figure 6 (before ageing).

In the lower graph, it can be seen the current distribution over the macro-cells for the aged device.

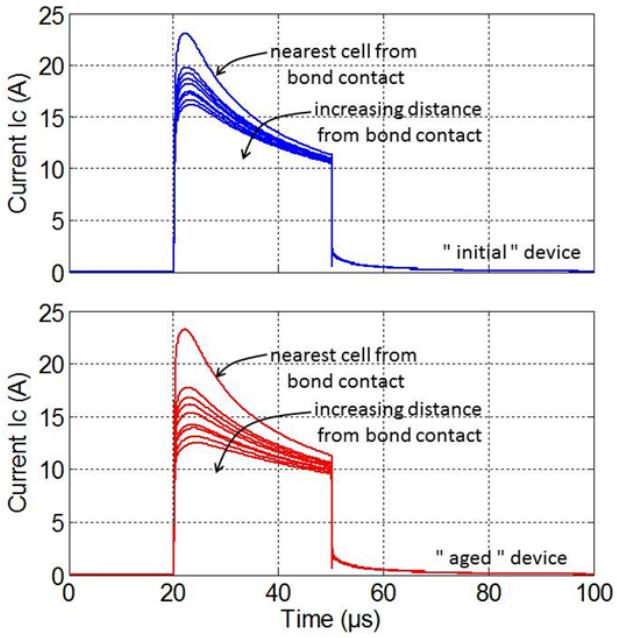


Figure 6. Macro-cell current distribution

As expected, we observe that the nearest cell from bond contact conducts the highest short-circuit current level.

Concerning the other cells, the current is shared in such a way that current level decreases with the distance of the corresponding macro cell from the bond contact.

This behavior is explained by the applied inner gate to source voltage in each macro-cell as shown in the upper graph of Figure 7a. The resistance access to each macro-cell is increased in the gate circuit from the closest to the farthest macro-cell from the bond contact. This explains the distribution of gate voltage over the cells

and consequently the short-circuit current distribution. The metallization ageing emphasizes this effect since its consequence is the increase of the distributed access resistance. So, it can be seen in the lower graphs of Figures 6 and 7a the amplification of these effects.

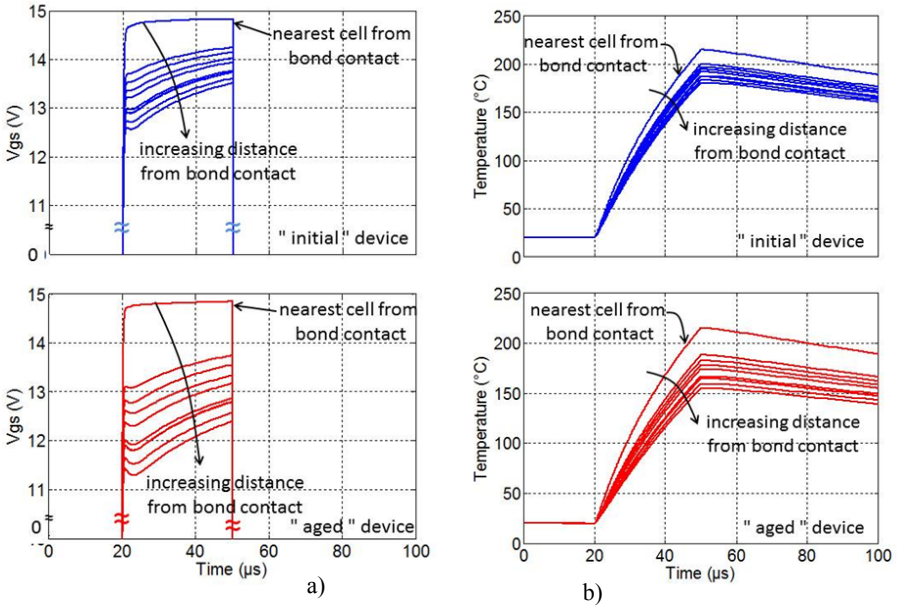


Figure 7. a) Macro-cell inner gate-to-source voltage distribution; b) Macro-cell temperature distribution

4.3. Effects on the temperature distributions

Temperature distributions inside macro-cells are given in the upper graph of Figure 7b for the "initial" device and in the lower graph for the "aged" one.

At the end of the simulated short-circuit, the temperature rises from 20°C (initial value) until 150°C to 215°C depending on the relative position of each macro-cell from bond contact. Naturally, the temperature distribution follows the current level distribution. We can observe that the ageing has no consequence for the nearest cell from bond contact but effects increase with the distance from the bond contact.

5. Dynamic latch-up failure during short-circuit operation

In previous works (Lefebvre *et al.*, 2005; Arab *et al.*, 2008), it has been shown that when IGBT devices are subjected to repetitive short-circuit operations, a cumulative damaging mechanism takes place which leads to an ageing effect and

finally to a failure. We experimentally observed that this failure systematically appears when trying to switch-off the collector current during the last short-circuit cycle. The destruction phenomenon looks like a dynamic latch-up. In the following, we propose by numerical analyzes, on one hand to show that the dynamic latch-up is possible in these conditions and on the other hand to analyze the possible role of metallization ageing in this phenomenon.

The dynamic latch-up conditions have been obtained by tuning the parasitic inductance (Lp) of the power circuit. By using a low value of Lp (10nH), the overvoltage is reduced and the parasitic elements are not triggered. In these conditions, short-circuit occurs normally, as it can be seen in Figure 5 for the "initial" or "unaged" device, in the previous section. The collector current distribution over the cells is given in the upper graph of Figure 6.

When using a sufficiently high value for Lp (30nH), at the beginning of the turn-off transient process, the collector current begins to fall before the latch-up occurs as shown in Figure 8a. This trend is clearly observed when the stray inductance is largely increased (Lp = 120nH), the collector current no longer follows the turn-off command and latch-up finally occurs (Figure 8b).

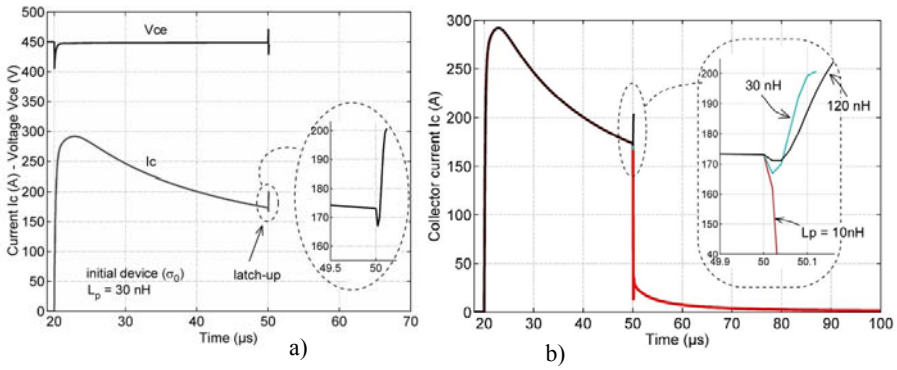
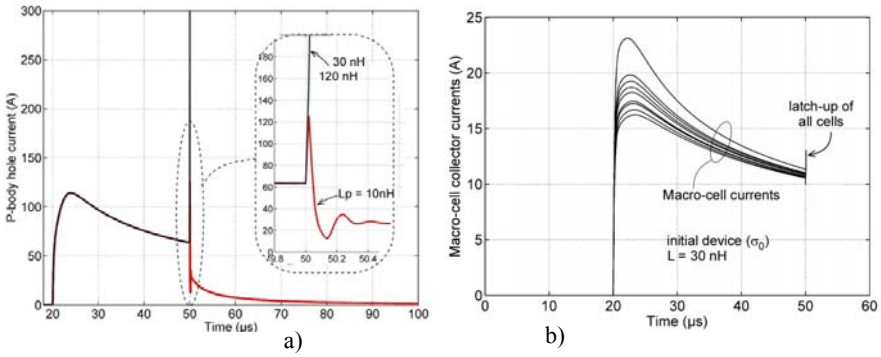


Figure 8. a) Lp = 30nH and "initial" device (latch-up); b) Collector current (IC) for different values of parasitic inductance (Lp = 10 nH, 30 nH to 120 nH)

It should be noted that the simulations show the strong dependence of the parasitic inductance Lp on the collector current (Ic) during switching operation especially during the turn-off. Thus, numerical analyses have shown that when current is switched-off, the transient evolutions of anode current (I_A) and channel current (I_{MOS}) have slight different dynamics. During transient, the electron current (I_{MOS}) switches more quickly than the collector current and consequently an additional flow of holes Ip (P-body hole current) can appear as shown in Figure 9a, in order to maintain the current law. So, high variations of this current may occur at this time. If the additional

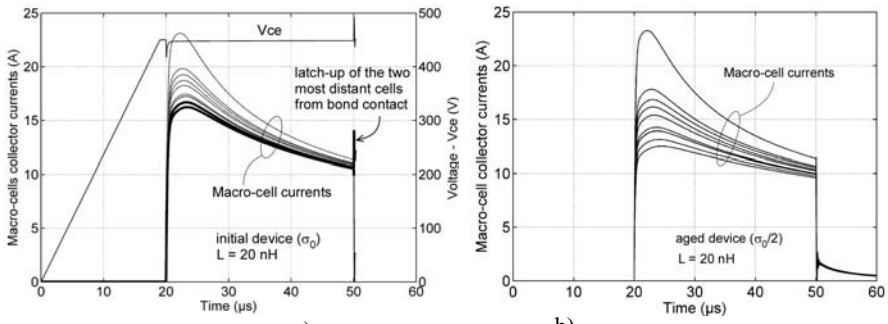
current is too high, it can trigger the npn parasitic transistor. This phenomenon can be amplified with a too high parasitic inductance Lp.



a) b)

Figure 9. a) P-body hole current (Lp=10nH, 30, and 120nH); b) Distributed currents for short circuit operation for Lp=30nH and "initial" device (latch-up)

In these conditions, the current distribution over the macro-cells is given in Figure 9b, where we can see that latch-up occurs for all cells with the use of a large Lp value (Lp = 30nH).



a) b)

Figure 10. a) Distributed currents for short circuit operation for Lp=30nH and "initial" device (latch-up); b) Short circuit operation for Lp=20nH and "aged"device (no latch-up)

Consequently, it should be possible to find an intermediate value of Lp, between these two values, in order to point out a critical latch-up conditions in which the macro-cells don't behave all in the same way at the very beginning of the latch-up process. Some of them may exhibit the phenomenon before others. If this "critical" condition can be found, one can highlight the trend when chip metallization ageing occurs. This "critical" short-circuit condition is that given in Figure 10a, where Lp is

20 nH. For this particular condition, one can see in this figure that, at the very beginning of the switch-off, only the two most distant cells from the bond contact trigger the parasitic transistor (bold lines) whereas the other ones don't. This situation leads finally to the failure.

As explained above, these "critical" latch-up conditions allow investigating the possible role of the chip metallization ageing. The aim is to confirm or disprove a hypothesis about the effect of the metallization on the observed failures in (Lefebvre *et al.*, 2005; Arab *et al.*, 2008). For this purpose, the preliminary results in Figure 10b show that in strictly identical conditions of Figure 10a with "aging" of the metallization by an increase of the resistivity ratio of 2, there is no latch-up.

So, these first results seem to indicate that the aging of the metallization is not responsible for the observed dynamic latch-up during short-circuit. Nevertheless, these preliminary results have to be confirmed by further analyzes.

6. Conclusion

In this paper, a distributed electro-thermal model at the power die level has been introduced to analyze the behavior of power electronic devices with the use of Simplorer software. The model consists on a 1D electro-thermal model for each macro-cell electrically connected by their terminals and a nodal 3D thermal RC network. This model has been used to evaluate the impact of the ageing of the metallization layer which is taken into account by an increase of its electrical resistivity. Simulation results show how temperature and current inhomogeneities increase within the power die with the metallization ageing. Simulation results confirm, for the first time, experimentally observed dynamic latch-up failure mode when trying to switch-off the short-circuit current. Numerical results suggest that the aging of the chip metallization is not responsible for the observed dynamic latch-up during short-circuit. Nevertheless, these preliminary results have to be confirmed by further analyzes.

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