

An Efficient Asymmetric Direct Current (DC) Source Configured Switched Capacitor Multi-level Inverter



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ABSTRACT

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This paper is dealing about Switched Capacitor Multi-Level Inverter (SCMLI) circuit which is controlled by triangular multicarrier Sinewave Pulse Width Modulation (SPWM) technique. The proposed SCMLI is powered from asymmetric DC source configuration to obtain multi-level output voltage by applying switching pulse to the main circuit from control circuit for switching operation. Fourteen switches and four capacitors are employing to do the proposed inversion operation in an effective way. Switching capacitors can perform boost operation to enhance voltage from the source level to the required level. Input DC from the asymmetric sources is converted to AC voltage for the application of consumers. This proposed conversion system is applicable for mainly in industrial and renewable energy-based energy conversion system because it can carry high output voltages. This proposed method gives about more efficiency. Also reduces switching losses in lower value, low conduction losses and capacitor ripple losses. The simulation model is analyzed in MATLAB/SIMULINK platform and the same validated in hardware results. The developed SCMLI structure is witness over other topologies for the power inversion process in the multi-level.

1. INTRODUCTION

At present, the inverters are playing a vital role in industrialized and in household applications [1]. Multilevel inverters are becoming workable DC-to-AC converting of power used for altered applications, like electrical drives, RECS applications, electric utilities, and filters [2]. For multiple application purposes a new SCMLI is developed [3]. For reliable working of inverters PWM techniques are preferable [4]. Another main drawback of conventional MLI is that they require extra supplementary circuit to maintain voltage as balanced at capacitors; this circuit amplifies its dimension, price and difficultness of converter [5]. Comparing with normal two-level inverters, the Multilevel Inverters shows many advantages, like producing synthesized output voltage, higher power production ability, low losses with high efficiency, less voltage strain across switching devices [6] those contains IGBTs, MOSFETs, power diodes, DC sources and capacitors [7]. In general, three usual Multi Level Inverter topologies are present, namely, Flying Capacitor (FC) Cascaded H-bridge (CHB) and diode clamped (DC) [8]. The latest Multi level inverter arrangement by way of more no. of steps linked by way of a small amount of power switching devices suggested [9]. The latest switched capacitor-diode structure is presented [10]. These sources can be the main for synthesized outputs [11]. It needs more capacitors in addition to as diodes on the way to generate heights levels of voltage at outputs [12]. On the way to defeat these problem supplementary circuits and composite controlling strategy has presented. The resonant switched capacitor converter is developed in this paper [13], which minimizes the capacitor voltage unbalance issues, drawbacks in amplify system as

bulky, pricey and difficulty lacking the remaining advantage of self-voltage boost ability.

On the way to attain self-voltage boost capacity and ease the unbalanced capacitor voltage issue exclusive of taking supplementary circuit, SCMLI is presented in this paper. Here, capacitors are used to be as alternative DC voltage sources. The SCMLI can produce multiple levels of voltage output with minimum number of power switches and sources. In count, SCMLI also enhance its source voltage up to required level of load voltage with alternating switching of those capacitors [14]. Another main benefit of SCMLI is obtaining of capacitor voltage balance with the help of switching sequence tactic. The remaining part of this paper is structured in the following pattern.

2. PROPOSED SCMLI

In this developed method, the capacitors of C_{11} with C_{11} can charge up to input voltage, while the capacitors of C_{12} & C_{12} can charge up to 4 times of input voltage with suitable triggering patterns. This indicates that the developed topology able to change the state of capacitors from charge and discharge simultaneously, that helpful to maintain voltage of capacitor at desired levels with lesser amount of voltage ripples. Figure 1 shows the developed SCMLI constructional details, which consists of 2 asymmetric DC voltage sources (V_i & $4V_i$), 14 unidirectional switching devices either IGBTs or MOSFETs, and 4 Switching capacitor devices. The entire arrangement makes 21 stages of output voltage levels with the load terminals.

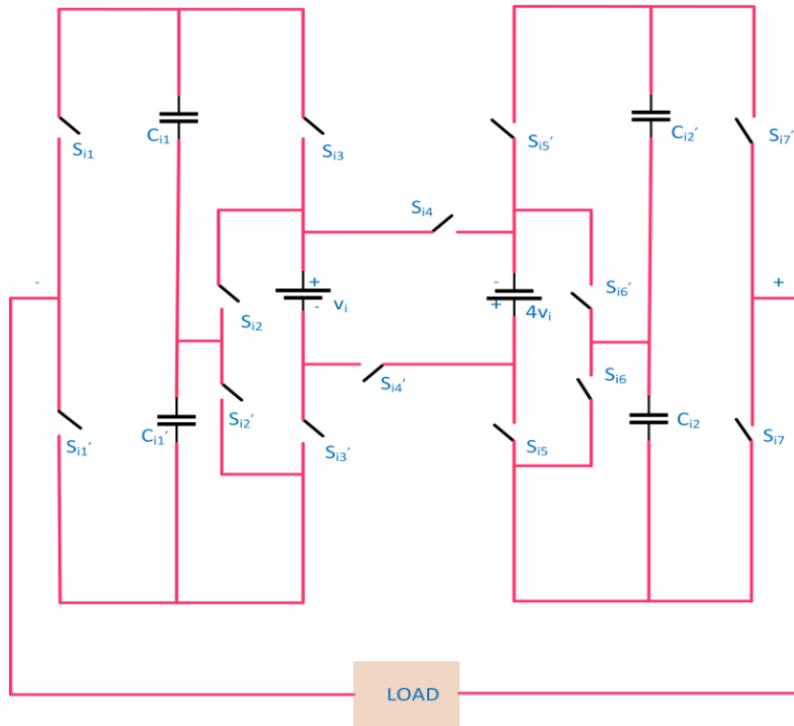


Figure 1. Developed SCMLI

2.1 Making a voltage level at zero

The output voltage at zero level was generated with turning ON the switches in the sequence of S_{11}' , S_{13}' , S_{14} , S_{15} , and S_{17} , the output voltage is appeared as zero in between load terminals. In this proposed topology, the capacitors C_{11} & C_{12} are arranged in charging condition by making a switch are turned ON in the pattern of S_{12} and S_{16}' in that order but capacitors which is connected to the circuit C_{11} & C_{12}' are operated in the position of non-conduction mode, as shown in Figure 2.

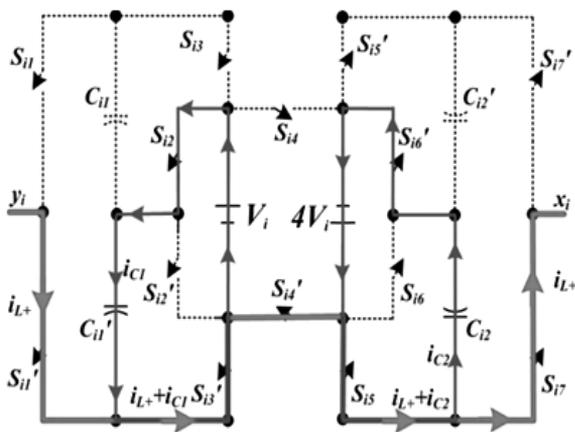


Figure 2. Equivalent circuit of zero level voltage

2.2 Making a voltage level at $\pm 2V_i$

The switching sequences are operated in the pattern of switches S_{11} ' to S_{17}' are switched ON, capacitor C_{11}' is associated with input voltage. Therefore, the voltage in between capacitor C_{11}' is additioned with input voltage and capacitor C_{11}' are operated in discharge mode, likewise it is shown inside Figure 3. Then load terminal output voltage nearly equivalent to 2 times of given input voltage. In this switching sequence,

capacitors are operated in charging condition by means of making turn on of switches S_{13} and S_{16} , respectively. In the same way, two times of negative input DC voltage will be implemented in between output terminals by connecting input source voltage with a capacitor C_{11} .

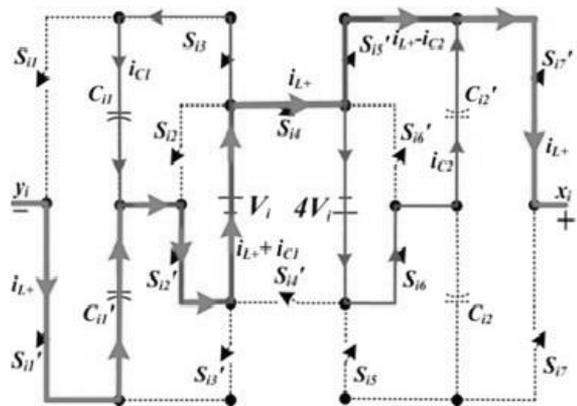


Figure 3. Equivalent circuit of ± 2 voltage level

2.3 Making a voltage level at $\pm 8V_i$ and $\pm 10V_i$

At the instant of $\pm 8V_i$ voltage level through connected load is provided by addition of supply voltage $4V_i$ with the capacitor voltage C_{12} and therefore, the capacitor is operated in discharging manner. Figure 4 shows the equivalent circuit of $\pm 8V_i$ voltage level for proposed topology.

This mode of operation is achieved by turning on switches in the sequence of S_{11} , S_{13} , S_{14} , S_{16} , & S_{17} . In this mode of operation, the capacitors C_{11} & C_{12}' are used in charging condition by using turned ON of power switches S_{12}' & S_{15}' correspondingly. The Figure 5 represents the equivalent circuit for $+10V$ level. When switching patterns are operated in the sequence of S_{11} ' to S_{15}' are switched ON, while the two capacitors are connected serially with supply voltage. Whereas

the charging capacitors are paralleled with input voltage of input voltage and $4V_i$, correspondingly therefore, in this mode, the output load voltage is summing up with supply voltages, those are almost equal to the voltage level of $+10V_i$. In the same way, $-10V_i$ is created by making turned ON the opposite switching pattern. Similarly, the remaining voltage levels also having various switching patterns. According to that only the SCMLI will operate and produce 21 level output voltage across the load.

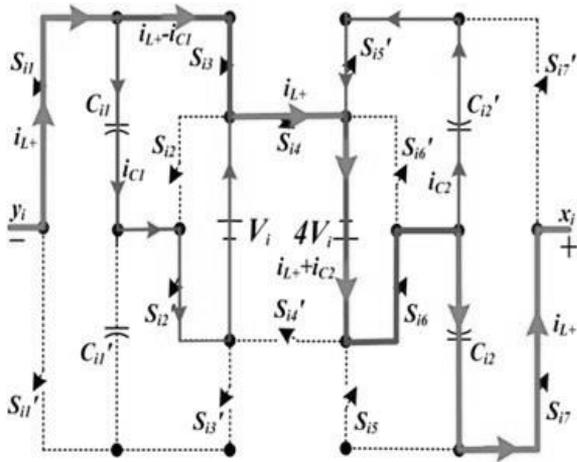


Figure 4. Equivalent circuit of ± 8 voltage level

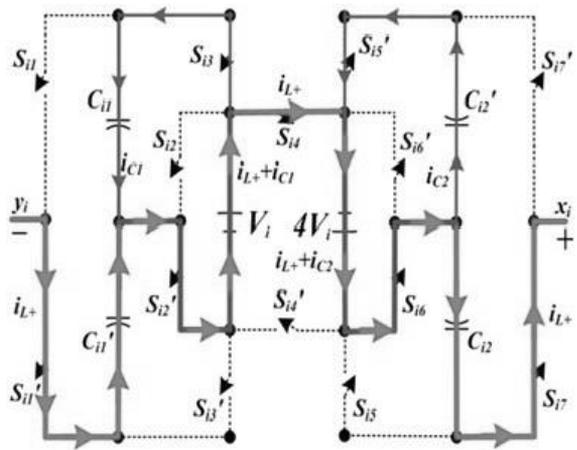


Figure 5. Equivalent circuit for ± 10 voltage level

3. MODULATION TECHNIQUE

These Pulse Width Modulation (PWM) techniques developed on the way to decrease the THD value of that load terminal voltage. Every variation on sinusoidal wave output load voltage are cause harmonic at load and this harmonic produce EMI, losses and pulsating torque occurs in electrical drives. However, the rising of switching frequency in PWM causes reduction of lower order harmonics by affecting the carrier switching frequency. The reference has maximum magnitude A_r and as well as frequency f_r . The operating principle of multi carrier SPWM is that comparing of triangular carrier signal with sinusoidal reference wave. When carrier signal is more compared to reference then relevant switch is ON and when reference signal is more compared to carrier then relevant switch is OFF. Generally, MLIs, the amplitude value of modulating index is M_a and modulating

frequency ratio M_f are shown in Eqns. (1) and (2).

$$M_a = \frac{A_r}{(m-1)A_c} \quad (1)$$

$$M_f = \frac{f_c}{f_r} \quad (2)$$

Here A_r and A_c are amplitude of reference and carrier wave in that order. Found f_r and f_c are frequencies of reference and as well as carrier wave correspondingly. Here modulation index value is taken as 0.98 for SCMLI for 14 power switches with different carrier signals.

3.1 Triangular multicarrier SPWM

The multicarrier modulation technique is used for multilevel inverter and multilevel inverters completed with the usage of some triangular waves as a carrier signal and single sine wave as a reference wave for each and every phase and carrier implemented Sub-Harmonic PWM (SH-PWM) that followed m no. of level inverter, $m-1$ no. of carriers of similar frequency f_c , identical magnitude A_c are liable such bands engage contiguously, which shows by usage of regular triangular carrier waves produce fewer harmonic distortions where output side of inverter. Now IPD technique is used. This IPD technique has better results than the other techniques. Figures 6 and 7 show the TMC SPWM technique of PD and IPD for the modulation index value of 0.8 and 1 respectively.

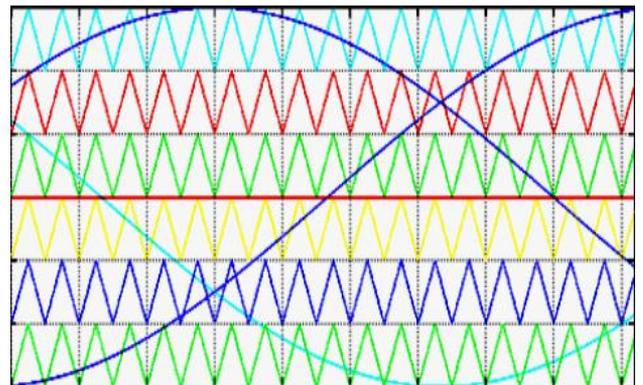


Figure 6. PD of TMC SPWM with modulation index value as 1

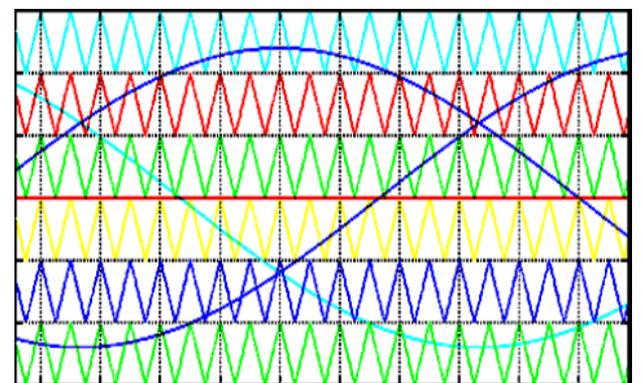


Figure 7. IPD of TMC SPWM with modulation index value as 0.8

4. POWER LOSS ANALYSIS

4.1 Efficiency

The losses in the developed SCMLI structure is mostly intense on three main power losses, specifically losses during switching (P_{sw}), losses during conduction (P_{con}), and losses with capacitor ripples (P_{ripple}). Then overall power loss (P_{loss}) of SCMLI is written as following:

$$P_{loss} = P_{sw} + P_{con} + P_{ripple} \quad (3)$$

The overall efficiency (η) of the developed inverter is given by the following Eq. (4):

$$\eta = \frac{P_{Out}}{P_{Out} + P_{Loss}} \quad (4)$$

4.2 Switching losses

The most common losses of power semiconductor switch take place whereas the switch is operated in transition condition. Whenever the switching pattern is distorted in the position ON state to OFF state and vice versa, once the linear estimation among the switch voltage and the switch current throughout the transition period t_{off} and t_{on} is measured, the total energy losses are happened in the i^{th} order power semiconductor switch is written as following expression:

$$E_{i,on} = \int_0^{t_{on}} V_{swi} \left(1 - \frac{t}{t_{on}}\right) I_i \left(\frac{t}{t_{on}}\right) dt = \frac{1}{6} V_{swi} I_i t_{on} \quad (5)$$

$$E_{i,off} = \int_0^{t_{off}} I_i \left(1 - \frac{t}{t_{off}}\right) V_{swi} \left(\frac{t}{t_{off}}\right) dt = \frac{1}{6} V_{swi} I_i t_{off} \quad (6)$$

where, I_i and I_i' are represented the switching current parameters, behind ON state and ahead of OFF states. To identify the power energy switching losses from the fundamental time period of the i^{th} order switch position, the amount of ON state conditions and OFF state transitions over a period can be evaluated. Hence, total energy power losses for one cycle period for the i^{th} order switch position is expressed by the following equation:

$$E_{i,sw} = (N_{ON,i} * E_{i,on}) + (N_{off,i} * E_{i,off}) \quad (7)$$

The total power switching losses of the i^{th} order switch over a cycle are illustrated by the equation,

$$P_{i,sw} = \frac{(N_{ON,i} * E_{i,on}) + (N_{off,i} * E_{i,off})}{T} \quad (8)$$

$$= \frac{1}{6T} V_{swi} I_i (N_{ON,i} t_{on}) + (N_{off,i} * t_{off})$$

The overall switching losses in terms of power value can be proposed SCMLI inverter is calculated as following:

$$P_{sw} = \sum_{i=1}^{14} P_{i,sw} \quad (9)$$

$$= \sum_{i=1}^{14} (N_{ON,i} * P_{i,on}) + (N_{off,i} * P_{i,off})$$

4.3 Conduction losses

The total conduction losses in this developed inverter arrangement is measured by the each and every element's internal resistance is considered for evaluation. From this investigation of the equivalent circuit the average power loss in conduction period in positive and as well as negative half cycles are same. The average power losses of conduction period for one full cycle are evaluated. During first positive voltage level, the total period is considered about the duration of $(t_2 - t_1)$ s in T (one full cycle). Therefore, the average loss of power during conduction for both first levels of load voltage given as following,

$$P_{ave1} = \frac{2(t_2 - t_1)}{T} (p_1 + p_{1-}) \quad (10)$$

The average power loss of the conduction period for remaining voltage levels are to be calculated based on Eq. (8). Thus, the average conduction losses for a cycle is expressed as following:

$$P_{con} = \sum_{j=1}^{10} P_{avej} \quad (11)$$

where, $j=1, 2, 3, \dots, 10$.

4.4 Capacitor ripple losses

These are arisen because of voltage variation among that capacitor and its relevant feeding source. Considering capacitor C_k is associated with discharging operation on behalf of a greatest time period $(t_{j+1} - t_j)$, subsequently highest voltage ripple of that consequent C_k is given in Eq. (12):

$$\Delta v_{ck} = \frac{1}{C_k} \int_{t_j}^{t_{j+1}} i_{ck}(t) dt \quad (12)$$

$i_{ck}(t)$ is capacitor's current during dis-charging. These currents are naturally similar to output terminal currents. Then capacitor ripple losses per one full cycle of capacitor C_k evaluated with following equation:

$$P_{ripck} = \frac{1}{2T} C_k (\Delta v_{ck})^2 \quad (13)$$

The overall ripple losses for each and every capacitor are named as C_{i1} , $C_{i1'}$, C_{i2} & $C_{i2'}$ for a full cycle is determined by following Eq. (13). Then entire capacitor ripple losses for one full cycle are given as following:

$$P_{ripple} = P_{ripci1} + P_{ripci1'} + P_{ripci2} + P_{ripci2'} \quad (14)$$

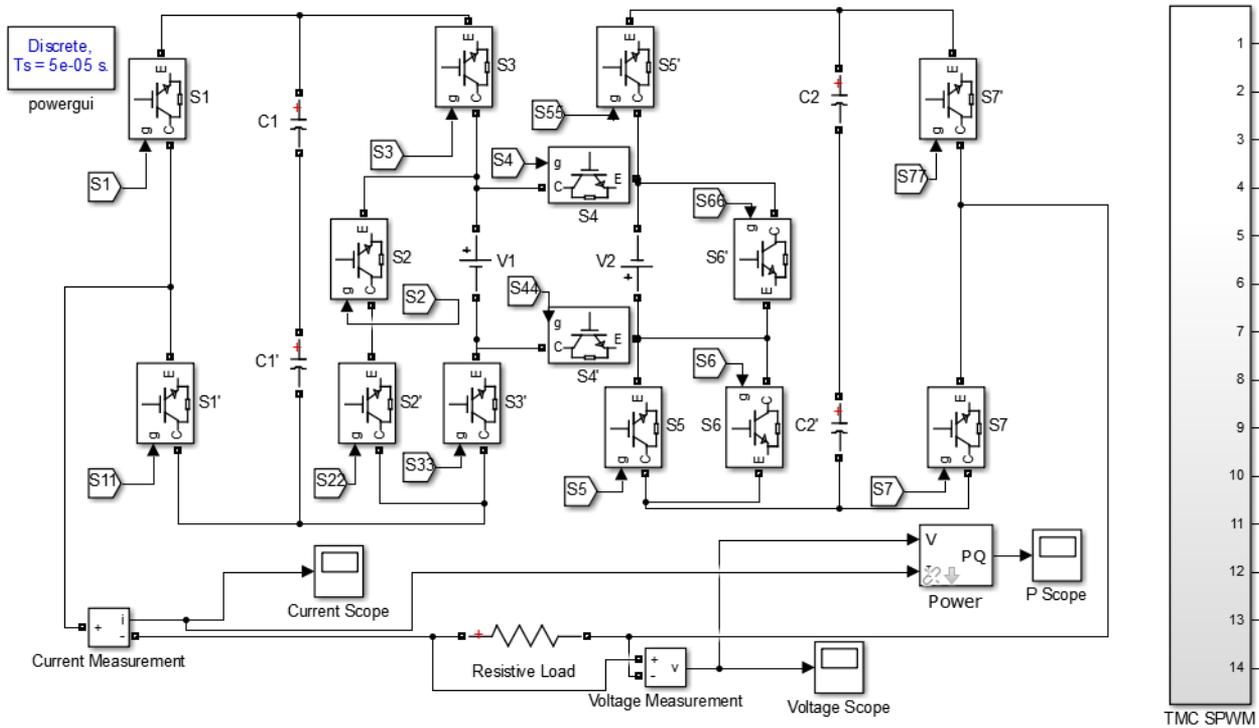


Figure 8. SIMULINK model

5. RESULT AND DISCUSSION

The Switched Capacitor Multilevel Inverter (SCMLI) model with triangular multi carrier SPWM is simulated in MATLAB software to demonstrate achievability of SPWM technique, which is shown in Figure 8. This proposed method gives about 96.02% of efficiency. Also reduces switching losses in lower value as 0.527 W, conduction losses as 4.69 W and capacitor ripple losses 0.0799 W.

This simulation model considered IGBTs as power switches devices and the simulation results of SCMLI are obtained, when 50ohms resistive load is connected. Figure 8 shows simulated model of developed SCMLI and that designed and simulated using MATLAB/SIMULINK software. In this case, the amplitudes of the DC input power supplies are considered as 100 V & 400 V. By connecting an input DC voltage sources, the developed topology be able to create a high output voltage of 1000 V. The load across the SCMLI is 50ohms corresponding to that the output current of SCMLI is 45.4 A. The output power of developed SCMLI is obtained 127.66 W. Therefore, all the capacitors are set as 560 μ F when the primary switching method is implemented; switching losses are noticeably a smaller amount. From the calculation switching losses are obtained as 0.527 W, capacitors ripple losses as 0.0799 W and Conduction losses as 4.69 W. Then overall losses in developed SCMLI are 5.296 W. By the observation capacitor ripple loss and switching losses are smaller than conduction losses. With the output power and losses, the efficiency can be calculated using Eq. (2). This developed SCMLI produces output voltage about 1000V and it is shown in Figure 9 and Figure 10 using with & without filter. The output 21-level voltage waveform at load terminals to be shown in the Figure 11 as load current, which is 45.4A and output power as 127.66kW as shown in Figure 12. Table 1 gives obvious detail about input and output parameters of proposed system.

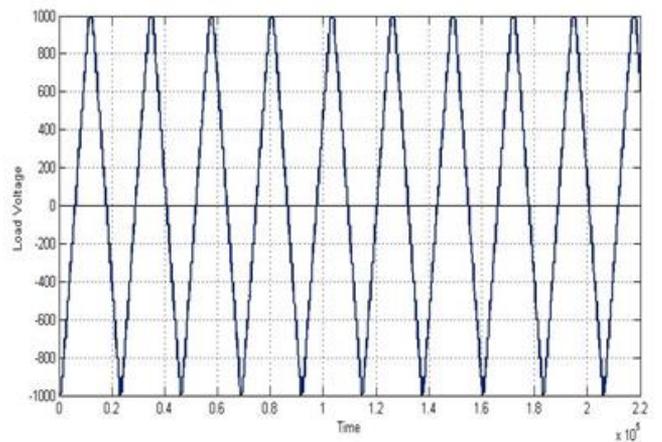


Figure 9. Voltage at load terminals without filter

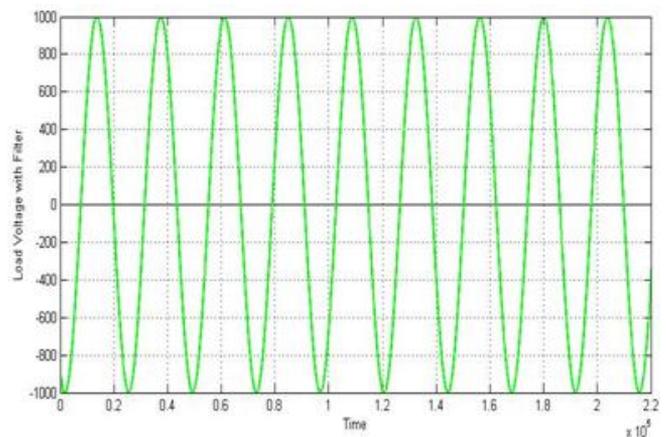


Figure 10. Voltage at load terminals without filter

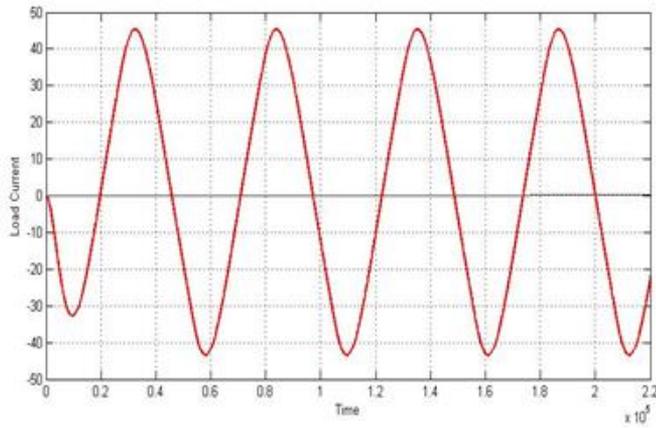


Figure 11. Load current waveform

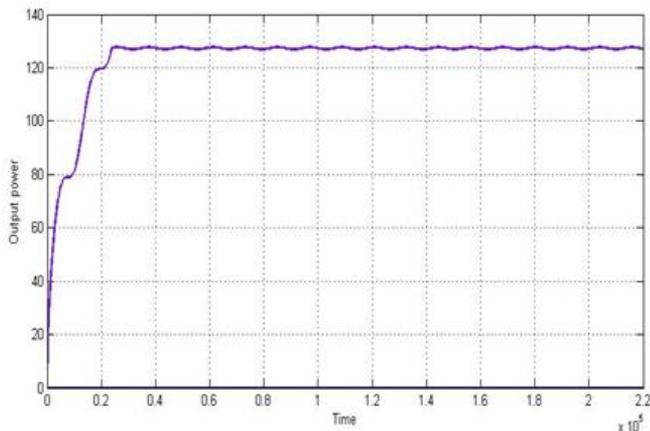


Figure 12. Output power waveform

Table 1. Input and output parameters of SCMLI

Parameters	Values
Input Voltages – Asymmetric Voltage	100 V, 400 V
Output Voltage	1000 V
Output Current	45.4 A
Output Power	127.66 kW
THD of output voltage without filter	8.34%
Peak fundamental load voltage without filter	858.5 V
THD of output voltage with filter	0.61%
Peak fundamental load voltage with filter	1002 V
THD of output Current	14.71%
Switching losses	0.527 W
Conduction losses	4.69 W
Capacitor ripple losses	0.0799 W
Overall Efficiency	96.02%

Figure 13 illustrates about the 21 level SCMLI hardware implantation. It consists of IGBT power switches, driver circuit, switching capacitor, drives transformer, resistive load and DSO. When DC input voltage is given by asymmetric DC voltage sources through 21 level SCMLI circuit, which converts sinusoidal voltage from filtering circuit. Figure 14 shows the FFT analysis of filtered output voltage, the THD value is reduced as 0.61%. While connecting a without filter circuit, it gives about 8.34% THD.

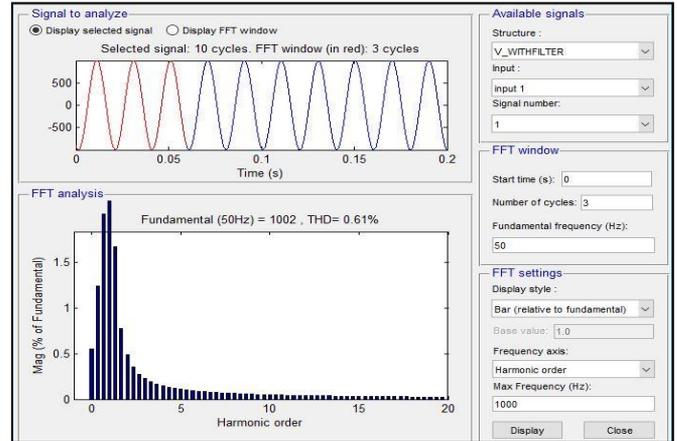


Figure 14. FFT analysis of a filtered output voltage

6. CONCLUSION

The Asymmetric DC Source configured SCMLI structure is developed and 21 output voltage levels across the load is carried out. Therefore, developed topology shows the potential to boosting of its source voltage and moreover, which provides considerably lesser losses than remaining topologies. It exhibits the efficiency of 96.02% and also compared with some topologies in several aspects like cost factor, no. of switching devices, no. of capacitors and etc. The proposed MLI is also applicable for high-voltage applications like industries as well as domestic purposes and RECS. Hence, it clearly justifies the developed SCMLI topology with Triangular Multi Carrier SPWM technique gives highly efficient than other topologies. It also has wide range of high voltage applications such as compensating devices in transmission, driving of electrical drives in industries and etc. Further this topology can be expended in different modulation technique to reduce power losses and improve overall efficiency.

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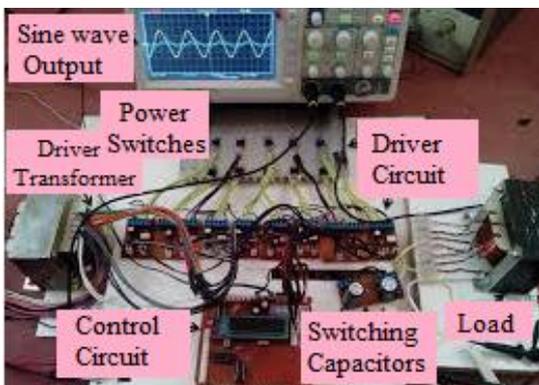


Figure 13. Hardware implementation

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