



## Fractional Order Sliding Mode Control Design for a Buck Converter Feeding Resistive Power Loads

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### ABSTRACT

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Standalone DC micro-grid requires highly efficient power converters with high performance robust controllers. This research work deals with the hardware implementation of a load side buck converter and its control system integrated in a DC micro-grid system. This paper presents a novel fractional order sliding mode control (FSMC) method for voltage regulation of a buck converter feeding a constant power load. FSMC controller is derived based on the average state space model of the buck converter and its stability is verified using Lyapunov theorem. Finally, the FSMC controller is implemented using Arduino mega 2560 processor and the obtained results are compared with classical sliding mode control (SMC), proportional, integral, derivative (PID) control and fractional order PID control system (FOPID) under constant and variable resistive loading.

## 1. INTRODUCTION

Direct current (DC) micro-grid is an emerging research topic in recent times. The advantages of the DC grids over alternative current (AC) grids include better reliability, power efficiency and simpler architecture [1]. Due to the recent advancements in power semiconductor technology and enhanced computational power of processors the DC distribution is becoming the most feasible solution for both the industrial and residential loads. AC grids are complex, and many vital parameters are required to be taken care for its proper operation. These include the power factor, reactive power compensations, frequency and phases. In comparison to the AC grids, DC distribution does not require the control of the above all parameters [2-4]. A 10kwatts experimental prototype for a DC micro-grid is presented in reference [5].

Later, several other researchers extended the idea and developed several other applications of the DC micro-grids such as power backup source for telecommunication systems [6], distributed generation [7], data centers [8], and consumer loads [9]. Based on the voltage levels, reliability, stability and standardization of the components, several topologies have been proposed for DC microgrids such as single bus topology [10, 11], multi bus topology [12, 13] and reconfigurable topology [14].

The stability study for the DC micro-grids under the constant power loading is another important research area and in the recent times many researchers are focused on the stability issues of the DC micro-grid integrated converters. The stability issues of micro-grid integrated DC-DC converters have been reported by Cupelli et al. [15], AL-Nussairi et al. [16] and Asghar et al. [17]. The stability issues are generally addressed using closed loop techniques and the details have been discussed by Asghar et al. [17]. Apart from the stability issues, feedback control system needs to be

carefully selected for optimal performance of DC micro-grids. DC micro-grids are interfaced through controllable power converters both at the source and load sides with a common DC link bus, thus voltage regulation is the control priority. To regulate DC link voltage for a micro-grid, the most widely utilized method is the droop control, which works on the cooperative sharing of the power or current among several converters [18, 19]. Droop control emulates a virtual resistance (VR) control loop along with the voltage loop [20, 21]. There are several limitations of the droop control method such as the load dependency in the voltage equation. The load dependency over the voltage causes a low efficiency of the current sharing algorithm. To solve this issue, secondary and tertiary controllers are proposed in the literature [3].

The droop control method limits the capability of the closed loop system in providing the desired coordinated performance of several components with different characteristics. Thus decentralized, centralized or distributed supervisory controllers are required to establish a specific mode such as droop control or maximum power point tracking (MPPT) [22, 23] or energy storage mode [24] should be adopted. Apart from the voltage and current regulation problem, stability of the DC micro-grid needs to be ensured over a wide range of operation. Points of load converters are tightly regulated, and it poses a challenge from the point of view of a negative impedance characteristic within the bandwidth of the applied control loops [25]. The negative impedance characteristic reduces the overall damping of the closed loop and it may lead to the instability of the whole system.

Apart from droop control schemes, several linear and nonlinear methods have been proposed for the control problem of DC micro-grids in the literature.

To design a linear control system, the model linearization technique is used for buck converter system [26]. Apart from its simple practical implementation, linear control methods

lack the ability of handling uncertainties and parameter variation. Moreover, the converter operating point depends on the small signal model parameters [27]. Due to the variation of the system parameters and large signal transient changes in the load, the above linear controllers are not able to ensure system stability [28]. Similarly proportional, integral and derivative (PID) controller fails to perform optimally because of the non-linear dynamics of the power converters; and especially for point of load converters [29].

Nonlinear controllers are capable for compensating the disturbances and uncertainties in the parameter with fast transient response. Some nonlinear control methods have been discussed in the literature such as fuzzy sliding mode control [30, 31], robust sliding mode control [32, 33], optimal control [34], feedback linearization [35], adaptive control [36, 37] and extended state observer based control [38, 39] for the DC-DC converter. All the cited methods above are integer order and there are few research articles reported on the non-integer (fractional order) control of DC microgrid integrated power converters.

Recently, fractional order control (FOC) has emerged as a new choice to control both linear and nonlinear systems. It utilizes the attributes of fractional integrals and derivatives in the control schemes. A brief theoretical analysis of fractional operators has been discussed by Delghavi et al. [40] and Matignon [41], whereas the tuning of FOC schemes has been explained by Aghababa [42] and Li and Deng [43] for achieving optimal controls performance.

Linear FOC control schemes have been proposed for buck converter system by Calderon et al. [44] and Monje et al. [45]. In comparison to integer order controllers, fractional order methods offer superior performance due to an extra degree of freedom. However, the FOC control schemes utilize high computational resources when implemented over processors. This statement is verified in an experimental study published recently [46]. Apart from linear FOC control schemes, several nonlinear non integer methods have also been reported in the literature. Stability of fractional order nonlinear systems is discussed by Li et al. [47] while a generalized approach for tuning and auto tuning of FOC controllers is proposed by Monje et al. [48]. By choosing suitable non integer sliding surfaces, the FOC controllers consume less memory and less power over processors [46].

Based on the above literature survey, this article formulates a novel fractional order sliding mode control (FSMC) for a point of load buck converter. The proposed controller is derived based on fractional order sliding manifold. The stability of the proposed control scheme is proved using Lyapunov theorem. The proposed control scheme is implemented using Matlab/Simulink and Arduino mega 2560 hardware. Finally, the comparison of the proposed FOSMC controller is done with classical SMC, PID and fractional order PID controllers (FOPID) controllers.

## 2. FRACTIONAL DERIVATIVES AND INTEGRALS DEFINITIONS

Fractional order calculus finds several interesting applications in applied mathematics branch especially where the integrals and differentiators are applied. Fractional order calculus is applied to convert the integer integrators and differentiators in to fractional ones of any complex or real order. Fractional order operator is symbolized by  ${}_a D_t^\alpha$  and it

can be defined as follows [45]:

$${}_a D_t^\alpha \cong D^\alpha = \begin{cases} \frac{d^\alpha}{dt^\alpha} & , R(\alpha) > 0 \\ 1 & , R(\alpha) = 0 \\ \int_a^t (d\tau)^{-\alpha} & , R(\alpha) < 0 \end{cases} \quad (1)$$

Here  $\alpha$  and  $t$  represents the operating limits,  $\alpha$  is the order of fractional operator and  $R$  is the real part of alpha. The fractional differentiator and integrator introduced by Riemann Liouville definition is given as follows [45]:

$${}_a D_t^\alpha f(t) = \frac{d^\alpha}{dt^\alpha} f(t) = \frac{1}{\Gamma(m-\alpha)} \frac{d^m}{dt^m} \int_a^t \frac{f(\tau)}{(t-\tau)^{\alpha-m+1}} d\tau \quad (2)$$

$${}_a D_t^{-\alpha} f(t) = I^\alpha f(t) = \frac{1}{\Gamma(\alpha)} \int_a^t \frac{f(\tau)}{(t-\tau)^{1-\alpha}} d\tau \quad (3)$$

In Eq. (3),  $\Gamma(\cdot)$  represents the Euler's gamma function and can be defined as follows:

$$\Gamma(x) = \int_0^\infty e^{-t} t^{(x-1)} dt, x > 0 \quad (4)$$

The fractional order derivative and integrator defined by Grunwald Letnikov method is given as:

$${}_a^{GL} D_t^\alpha f(t) = \lim_{h \rightarrow 0} \frac{1}{h^\alpha} \sum_{j=0}^{[(t-\alpha)/h]} (-1)^j \binom{\alpha}{j} f(t-jh) \quad (5)$$

## 3. SYSTEM MODELLING

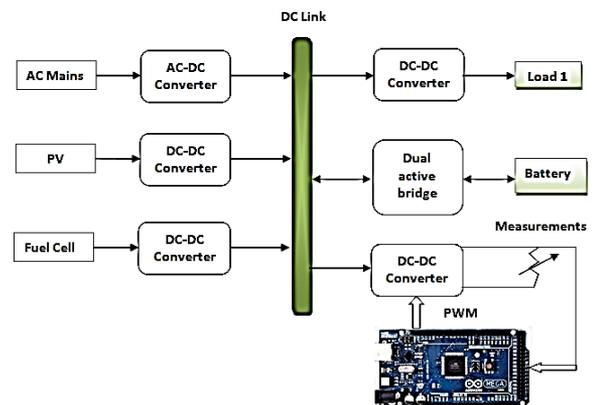


Figure 1. DC micro-grid block diagram

Block diagram of a DC micro-grid is given in Figure 1. The micro-grid consists of sources such as photo-voltaic (PV), fuel cell and AC grid. Each source is integrated to the DC link via source side converters. Similarly, loads are driven using load

side converters. Moreover, the battery storage system is integrated to the DC link via a dual active bridge. DC link is used to store and supply instantaneous energy from the source and to the loads respectively. As shown in the block diagram, the scope of this work to test the proposed controllers for a load side converter that drives a variable resistive load.

To derive the fractional order robust control system, it is necessary to derive an average state model of the system as a first step. By following the standard concepts of the switched mode power converters, the operation of the buck converter is divided in to two states. Figure 2 shows circuit diagram of a buck converter.

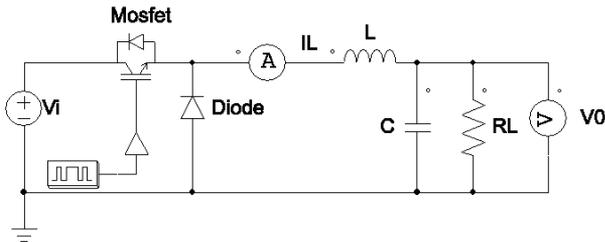


Figure 2. Circuit diagram of buck converter

Overall there are two states of the Mosfet switch. It can either be opened or in closed state. Thus, based on the two switching states, two equations are derived that represent the dynamics of the system. Consider the following two cases:

**State 1: When the Mosfet switch is closed**

When the Mosfet conducts then the converter dynamics are expressed as follows:

$$V_i = L\dot{I}_L + V_0 \quad (6)$$

$$C\dot{V}_0 = I_L - \frac{V_0}{R_L} \quad (7)$$

**State 2: When the Mosfet switch is open**

When the Mosfet switch is open so no current flows from voltage source, then the stored energy in the inductor coil is released through the freewheeling diode and the system dynamics are represented as follows:

$$L\dot{I}_L = -V_0 \quad (8)$$

$$C\dot{V}_0 = I_L - \frac{V_0}{R_L} \quad (9)$$

Here  $V_i$  represents the input voltage,  $V_0$  is the output voltage,  $I_L$  is the inductor current,  $L$  represents the inductance,  $C$  represents the capacitance and  $R_L$  is the load.

The average state space model of the buck converter is derived as following [21]:

$$L\dot{I}_L = uV_i - V_0 \quad (10)$$

$$C\dot{V}_0 = I_L - \frac{V_0}{R_L} \quad (11)$$

Taking into account the parametric uncertainties of the system, the system of Eq. (11) is further elaborated as follows:

$$\begin{aligned} \frac{d}{dt} I_L &= \frac{uV_i}{L} - \frac{V_0}{L} + d_i \\ \frac{d}{dt} V_0 &= \frac{I_L}{C} - \frac{V_0}{R_L C} + d_v \end{aligned} \quad (12)$$

The terms  $d_i$  and  $d_v$  represent parametric and load uncertainties in the power stage parameters represented as follows:

$$\begin{aligned} d_v &= \frac{uV_i}{\Delta L} - \frac{V_0}{\Delta L} \\ d_i &= \frac{I_L}{\Delta C} - \frac{V_0}{\Delta R_L \Delta C} \end{aligned} \quad (13)$$

The uncertainties in power stage parameters  $L/C$  and load perturbations can occur due various reason such as: (a) aging effect of the converter due to its prolonged operating time, (b) thermal effects; as the parameters are directly effected by the change in temperature (c) load variations  $\Delta R_L$ .

#### 4. CONTROLLER FORMULATION

In this section FSMC law is derived using system of Eq. (12). A fractional order sliding surface  $S_V$  is defined as follows:

$$S_V = c_1 D^{-\alpha} (V_r - V_0) + c_2 \int (\dot{V}_r - \dot{V}_0) \quad (14)$$

In Eq. (14),  $c_1, c_2$  represents the sliding surface constants,  $V_r$  shows the reference voltage command and  $V_0$  is the output voltage. By taking the fractional order derivative  $D^\alpha$  on both sides of Eq. (14), one obtains the following relation [42]:

$$D^\alpha S_V = c_1 (e_V) + c_2 D^{\alpha-1} (\dot{e}_V) \quad (15)$$

Here  $e_V = V_r - V_0$ , while its first derivative is expressed as follows:  $\dot{e}_V = \dot{V}_r - \dot{V}_0$ . Expanding Eq. (15) in terms of the capacitor voltage dynamics, the resultant expression is given by Eq. (16).

$$D^\alpha S_V = c_1 (e_V) + c_2 D^{\alpha-1} \left\{ \dot{V}_r - \left( \frac{I_L}{C} - \frac{V_0}{R_L C} + d_v \right) \right\} \quad (16)$$

Using Eq. (16), the current reference  $I_{L-ref}$  can be generated as follows:

$$I_{L-ref} = \frac{C}{c_2} \left\{ c_2 \frac{V_0}{R_L C} + \dot{V}_r + D^{1-\alpha} (K_1 S_V + c_1 e_V) \right\} \quad (17)$$

A current sliding surface  $S_I$  is defined as follows:

$$S_I = c_3 D^{-\alpha} (I_{L-ref} - I_L) + c_4 \int (\dot{I}_{L-ref} - \dot{I}_L) \quad (18)$$

In Eq. (18),  $c_3, c_4$  are the current sliding surface constants, and  $I_L$  is the inductor current. By taking the fractional order derivative  $D^\alpha$  on both sides of Eq. (18), one obtains the following relation:

$$D^\alpha S_I = c_3 (e_I) + c_4 D^{\alpha-1} (\dot{e}_I) \quad (19)$$

Here  $e_I = I_{L-ref} - I_L$  is the current error, while its first derivative is expressed as follows:  $\dot{e}_I = \dot{I}_{L-ref} - \dot{I}_L$ .

By including the dynamics of inductor current, Eq. (19) is further expanded as follows:

$$D^\alpha S_I = c_3(e_I) + c_4 D^{\alpha-1} \left\{ \dot{I}_{L-ref} - \left( \frac{uV_i}{L} - \frac{V_0}{L} + d_i \right) \right\} \quad (20)$$

The current control law is derived as follows:

$$\begin{cases} u = u_{eq} + u_s \\ u_{eq} = \frac{L}{V_i} \left\{ D^{1-\alpha} \left( \frac{c_3}{c_4} e_I \right) + \frac{V_0}{L} + \dot{I}_{L-ref} \right\} \\ u_s = \frac{L}{V_i} \left\{ D^{1-\alpha} \left( \frac{K_2}{c_4} \text{sgn}(S_I) \right) \right\} \end{cases} \quad (21)$$

In Eq. (21),  $K_1$  and  $K_2$  represent the control system constants.

#### 4.1 Stability proof

A Lyapunov theorem given by Aghababa [42] is utilized to prove the closed loop stability with the proposed control scheme. The overall system's stability will be proved in two steps. In the first step voltage loop is analyzed followed by the current loop. The following theorem is utilized to prove the stability.

**Theorem 1:** The proposed FSMC controller derived in Eq. (17) and (21) for the system given in Eq. (12) is stable if the following inequality holds true [18]:

$$\left| \sum_{j=1}^{\infty} \frac{\Gamma(1+\alpha)}{\Gamma(1-j+\alpha)\Gamma(1+j)} D^j S_V D^{\alpha-j} S_V \right| \leq \Omega_1(S_V) \quad (22)$$

Here  $S_V$ , represents the voltage sliding surface and  $\Omega_1(\cdot)$  is a positive constant.

#### 4.2 Proof for voltage loop

To prove the stability of the voltage loop, the Lyapunov candidate function is defined as follows:

$$V_V = \frac{1}{2} S_V^2 \quad (23)$$

Applying  $D^\alpha$  to Eq. (23) yields the following expression [42]:

$$D^\alpha V_V = S_V D^\alpha S_V + \left| \sum_{j=1}^{\infty} \frac{\Gamma(1+\alpha)}{\Gamma(1-j+\alpha)\Gamma(1+j)} D^j S_V D^{\alpha-j} S_V \right| \quad (24)$$

Eq. (24) is simplified by mixing it with Eq. (16) and Eq. (22):

$$D^\alpha V_V \leq S_V (c_1(e_V) + c_2 D^{\alpha-1} \left\{ \dot{V}_r - \left( \frac{I_r}{C} - \frac{V_0}{R_L C} + d_v \right) \right\}) + \Omega_1(S_V) \quad (25)$$

Combine Eq. (17) and Eq. (25), one obtains the following expression:

$$D^\alpha V_V \leq S_V (c_1(e_V) + c_2 D^{\alpha-1} \left\{ \dot{V}_r - \left( \frac{1}{C} \left( \frac{c_2}{R_L C} + \dot{V}_r \right) + D^{1-\alpha} (K_1 S_V) + c_1 e_V \right) \right\} - \frac{V_0}{R_L C} + d_v) + \Omega_1(S_V) \quad (26)$$

Further simplification of Eq. (26), yields the following expression:

$$D^\alpha V_V \leq -K_1 S_V^2 + d_v + \Omega_1(S_V) \quad (27)$$

By letting  $K_1 > |d_v| + \Omega_1(S_V)$  it is easy to show that  $D^\alpha V_V \leq 0$  that satisfies the reaching condition of sliding surface and  $S_V = 0$ .

#### 4.3 Proof for current loop

A Lyapunov candidate function is used to prove the current loop stability and it is given as follows:

$$V_I = \frac{1}{2} S_I^2 \quad (28)$$

Applying  $D^\alpha$  to Eq. (28) yields the following expression [42]:

$$D^\alpha V_I = S_I D^\alpha S_I + \left| \sum_{j=1}^{\infty} \frac{\Gamma(1+\alpha)}{\Gamma(1-j+\alpha)\Gamma(1+j)} D^j S_I D^{\alpha-j} S_I \right| \quad (29)$$

Eq. (29) is simplified by utilizing Eq. (20) as follows:

$$D^\alpha V_I \leq S_I (c_3(e_I) + c_4 D^{\alpha-1} \left\{ \dot{I}_{L-ref} - \left( \frac{uV_i}{L} \right) \right\} - \frac{V_0}{L} + d_i) + \Omega_2(S_I) \quad (30)$$

Here  $S_I$  represents the voltage sliding surface and  $\Omega_2(\cdot)$  is a positive constant. By combining Eq. (21) and Eq. (30), one obtains the following expression:

$$D^\alpha V_I \leq S_I (c_3(e_I) + c_4 D^{\alpha-1} \left\{ \dot{I}_{L-ref} - \left( \frac{V_i}{L} \left( \frac{L}{V_i} \left( D^{1-\alpha} \left( \frac{c_3}{c_4} e_I \right) + \frac{V_0}{L} + \dot{I}_{L-ref} \right) + D^{1-\alpha} \left( \frac{K_2}{c_4} \text{sgn}(S_I) \right) \right) \right\} - \frac{V_0}{L} + d_i) \right\} + \Omega_2(S_I) \quad (31)$$

Further simplification of Eq. (31), yields following expression:

$$D^\alpha V_I \leq -K_2 |S_I| + d_i + \Omega_2(S_I) \quad (32)$$

By letting  $K_2 > |d_i| + \Omega_2(S_T)$  it is easy to show that  $D^\alpha V_T \leq 0$  which means that reaching condition of sliding surface is satisfied and  $S_T = 0$ .

### 5. EXPERIMENTAL SETUP AND RESULTS

The proposed control scheme is implemented on Arduino mega 2560 for a DC micro-grid integrated buck converter as shown in Appendix B. Rapid control prototyping is utilized to program Arduino microcontroller from the Simulink environment as shown in Appendix A. The experiment is carried out under fixed load and also under load variations. The results obtained with proposed control scheme are than compared with classical SMC, PID and Fractional order PID controllers (FOPID). The control parameters are tabulated in Table 1 and Table 2, respectively.

**Table 1.** PID controller parameters

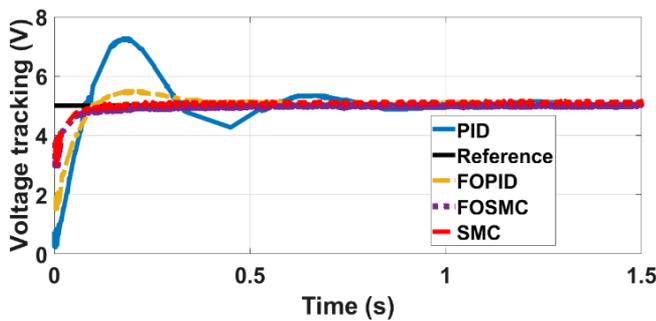
Controller	Kp	Ki	Kd	$\alpha$
PID voltage loop	10	30	0.5	0
PID current loop	5	12	0.5	0
FOPID voltage loop	2	10	0.1	0.85
FOPID current loop	1.5	5	0.1	0.85

**Table 2.** FSMC controller parameters

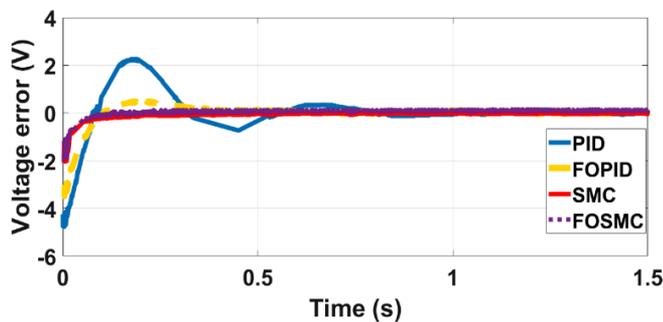
Controller	c1	c2	c3	c4	K1	K2	$\alpha$
PID voltage loop	5	2.5	3.2	1.3	0.5	1.25	0.2

#### 5.1 Voltage tracking under fixed load condition

Figures 3 and 4 show the voltage tracking and voltage error response of the system with different controllers under no load condition.



**Figure 3.** Voltage tracking response under fixed load



**Figure 4.** Voltage tracking error response under fixed load

The comparison of the voltage regulation response of the system under PID, FOPID, SMC and FSMC controllers are shown in Figure 3. The reference command signal is set to 5v. From the experimental results presented; the comparative data is tabulated in Table 3. From the results collected, it is concluded that the robust FSMC offers the desired performance in terms of rise time, settling time and steady state error when the system is connected to the fixed resistive load.

**Table 3.** Voltage tracking response

Controller	Rise time (ms)	Settling time (ms)	Steady state error	Overshoot (%)	Peak voltage
PID	13.491	982.9	2.25	47.08	7.251
FOPID	14.8	219.4	0.478	10.3	5.47
SMC	7.499	35.6	0.059	1.94	0.59
FSMC	7.199	33.6	0.049	1.74	0.49

#### 5.2 Voltage tracking response under load variations

In this section, the voltage tracking performance of the buck converter under load variations is compared with PID, FOPID, SMC and FSMC controllers. Reference command signal is selected as 5v. Initially a fixed 5 ohms resistive load is connected at the output of the buck converter. To check the robustness of all the above mentioned control schemes, two more resistors each carrying 5 ohms resistance are switched in parallel to the nominal load at  $t = 3$ sec and then switched off at  $t = 5$ sec. The voltage regulation and error response of buck converter system with PID, FOPID, SMC and FSMC controllers is shown in Figures 5 and 6 respectively. By observing the response of the system in all these cases between the time span between  $t = 3$ sec to 5sec, the following data points are collected.

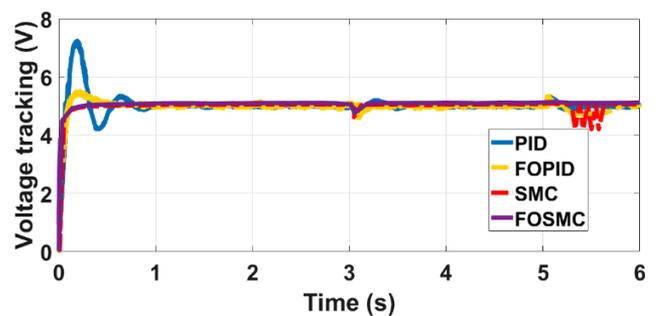
**For PID:** The maximum error recorded is +0.21v to -0.3v. The steady state error is approaching zero at 3.5 sec and 5.4 sec respectively.

**For FOPID:** The maximum error recorded is +0.3v to -0.4v. The steady state error is approaching zero at 3.25 sec and 5.3 sec.

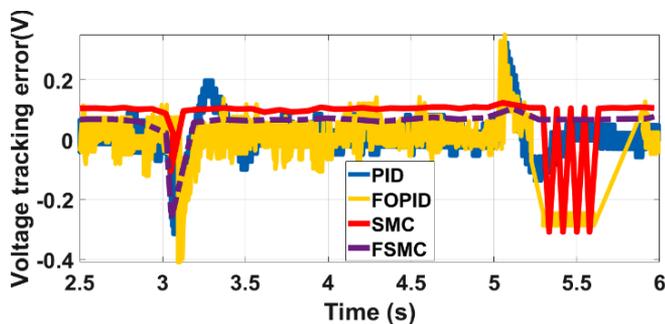
**For FSMC:** The maximum error recorded is +0.1v to -0.2v. The steady state error is approaching zero at 3.08 sec and 5.08 sec.

**For SMC with saturation function:** The maximum error recorded is +0.1v to -0.25v. The steady state error is approaching zero at 3.18 sec and 5.18 sec.

From the data comparison presented above it is concluded that in the case of FSMC, the system states returns to steady state in the shortest time after when the system is subject to the load variations.

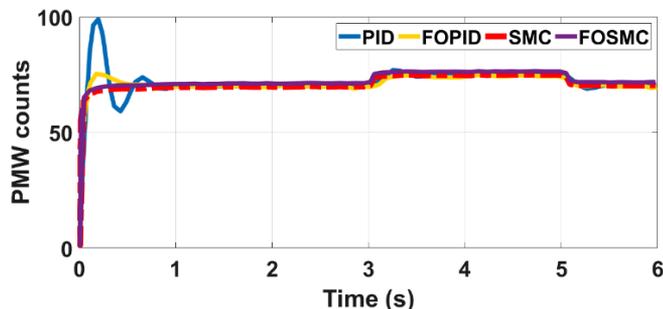


**Figure 5.** Voltage tracking response under load variations

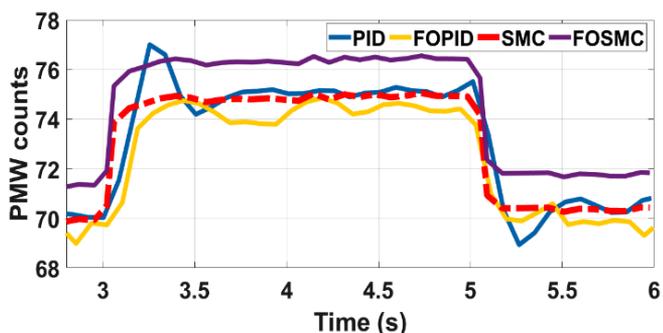


**Figure 6.** Voltage tracking error response under load variations

Apart from the system response with load variations, the transient response of the system under all variants of control schemes is shown in Figure 5. By noting the voltage tracking response from time  $t=0$  to 2 seconds, system with PID controller exhibits the largest error of +2v and -1v on both positive and negative sides of zero line, and also the settling time is around 1.5 sec. Similarly system with FOPID controller shows transient error of +1v and with improved settling time. From Figure 5, it is noted that FSMC controller shows superior transient and steady state performance under load variations.



**Figure 7.** Control excitation response under load variations



**Figure 8.** Enlarged view of control signal under load variations

Figures 7 and 8 show the recorded control signal excitations for all variants of the discussed controllers. The control signal excitation is represented as pulse width modulation (PWM) register counts. Transient response of the control excitations for all variants of the discussed controllers is clear from Figure 7. In the event when load is varied, the enlarged view of the control excitations is shown in Figure 8. From the presented results it is clear that FSMC takes maximum counts of 76 and thus it gives the best transient and steady state response as obvious from Figures 5 and 6.

## 6. CONCLUSION

Fractional order sliding mode controller is derived and implemented for a DC micro-grid integrated buck converter system. The controller is tested under ideal and variable load conditions. From the results it is concluded that fractional order sliding mode controller offers superior performance in terms of rise time, settling time and percent overshoot as compared to classical SMC, PID, and fractional order PID controllers. In future the proposed control method will be studied with respect to the computational resource requirements when it is implemented over the microprocessor. Moreover different methods and modifications will be suggested to minimize its computational resource utilization for practical implementation over a microprocessor.

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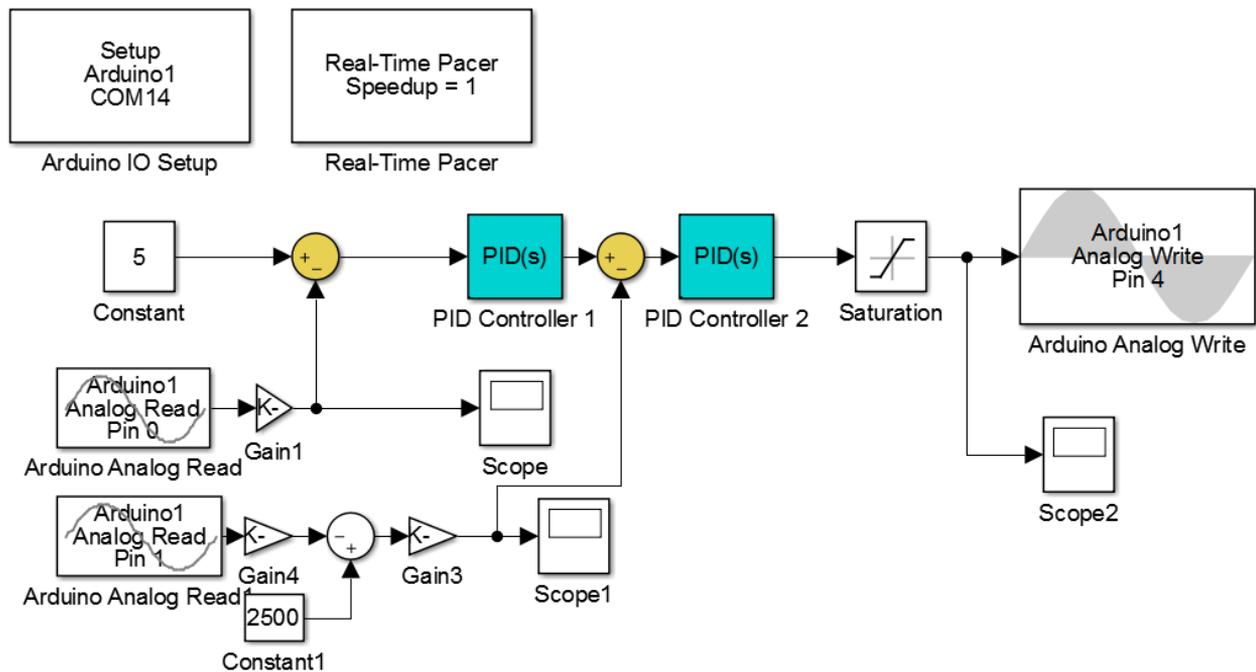
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#### APPENDIX A: Simulink Block Diagrams



**Figure A.1.** PID based buck converter Simulink block diagram

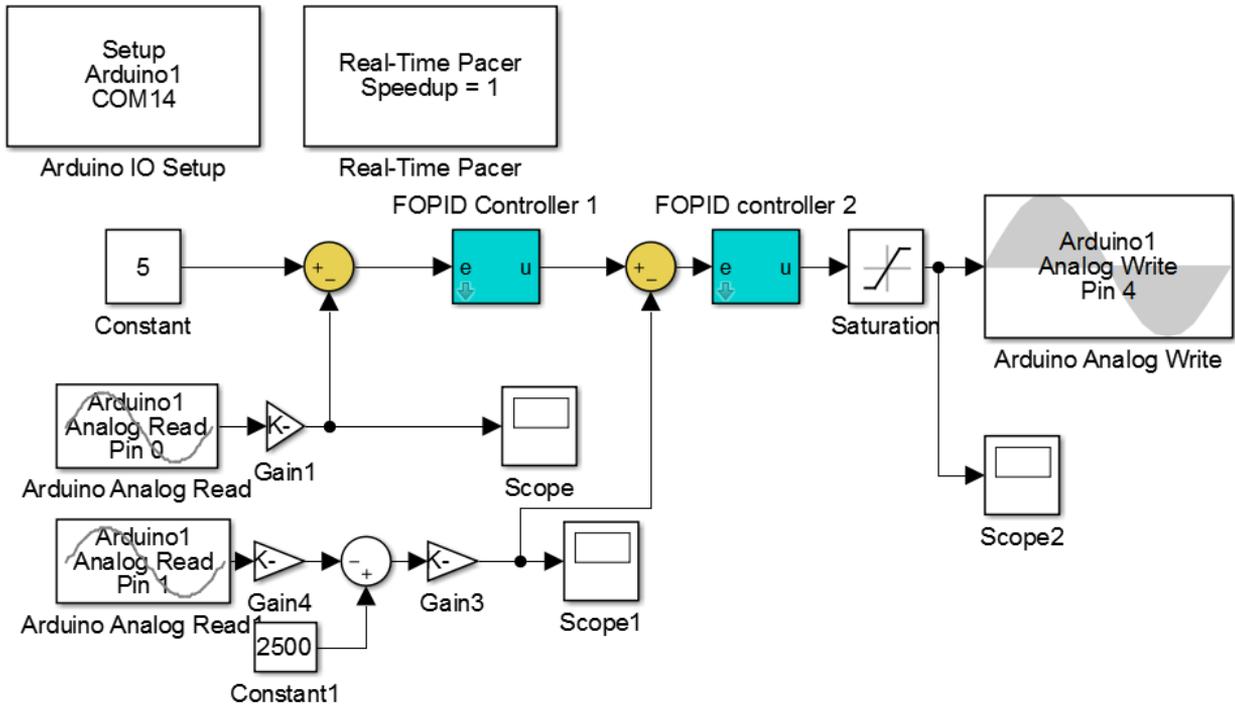


Figure A.2. FOPID based buck converter Simulink block diagram

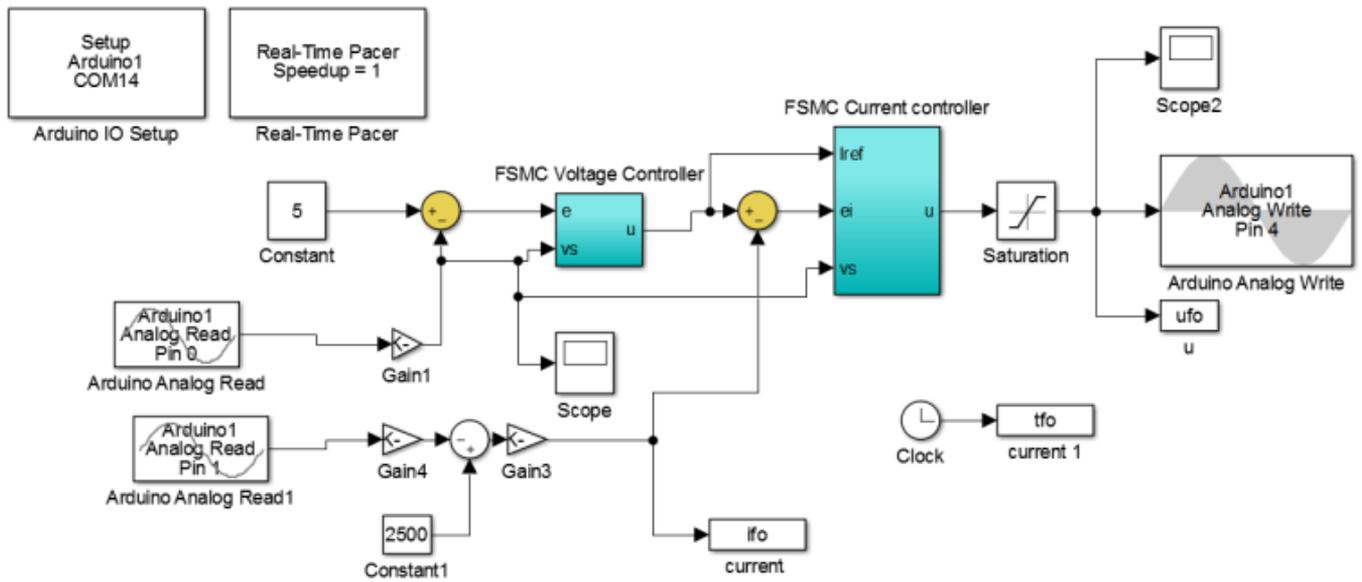


Figure A.3. FSMC based buck converter Simulink block diagram

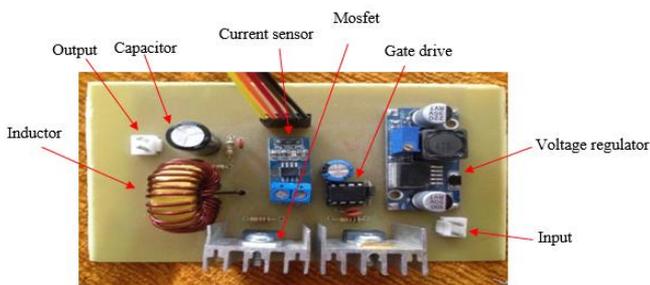


Figure A.4. Buck converter

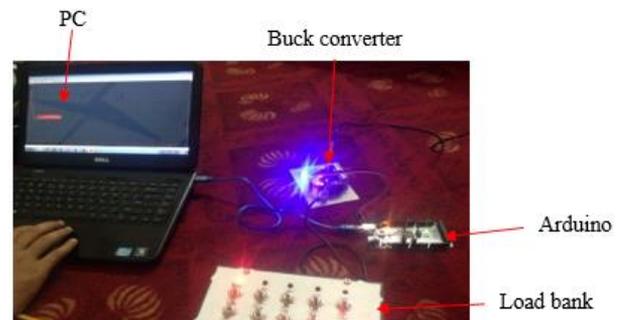


Figure A.5. Experimental arrangement

## Appendix B

**Table B1.** Buck converter and load bank parameters

Parameter	Value	Unit
Source Voltage ( $V_i$ )	18	Volt
Output Voltage ( $V_o$ )	5	Volt
Switching frequency ( $F_{sw}$ )	$62.5 * 10^3$	Hz
Inductor	$32 * 10^{-6}$	Henry
Capacitor (C)	$1000 * 10^{-6}$	Farad
Power	50	Watt
Load current (maximum)	10	Ampere
Current ripple ( $I_{ripple}$ )	18 %	Ampere
Voltage ripple ( $V_{ripple}$ )	$8 * 10^{-3}$	Volt
Total time ( $\Delta T$ )	$4.4 * 10^{-3}$	Second
Load bank	Four,5 ohms resistors are connected in parallel. Load changes are reflected by switching several resistors in parallel or disconnecting it	ohms