AMSE JOURNALS-AMSE IIETA publication-2017-Series: Advances C; Vol. 72; N°4; pp 227-247
Submitted Feb. 2017; Revised June. 2, 2017, Accepted July 15, 2017
https://doi.org/10.18280/ama_c.720403

Harmonic Compensation in Five Level NPC Active Filtering: Analysis, Dimensioning and Robust Control Using IT2 FLC

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Abstract

Shunt Active Power Filters (APF) are complex power electronics equipments adopted to compensate for current harmonic pollution in power systems. Using a proper capacitor as energy reservoir, the shunt APF purpose is to inject in the line grid currents cancelling the polluting harmonics. The performance of APF is principally depends on the voltage control algorithms for DC-side and the selection of reference current extraction methods. In controlling non-linear systems, uncertainty is one of the most difficult obstacles. For that reason, several reported results have shown that Interval Type-2 Fuzzy Logic Controllers (IT2 FLCs) are very interesting to handle uncertainties. In this current paper a new control technique of dc-link capacitor voltage in five-level NPC shunt APF based on IT2 FLC is established. The control performances on global system are showed under various settings. All series of simulation results in MATLAB/Simulink environment are demonstrated and compared to illustrate the effectiveness of this scientific research.

Key words

Shunt Active Power Filter (SAPF), Synchronous Reference Frame (SRF), Neutral Point Clamped (NPC), IT2 FLCs, Hysteresis Current Control (HCC), Total Harmonic Distortion (THD).

1. Introduction

The deteriorating quality of electric power is mainly caused by the widespread use of power electronic appliances in power systems [1], [2]. In three phase systems, harmonics component is a very serious and a harmful problem, it could also cause unbalance and excessive neutral currents [3]. Hence, it is necessary to reduce the mains harmonics below the limit specified in IEEE 519 harmonic standards.

Currently, APF have been widely investigated for the compensation of harmonics in power system. These filters are classified into shunt APF, series APF, hybrid filters (parallel passive filter and series APF) and finally, unified power quality conditioner UPQC (series APF and shunt APF) [4], [30]. An active filter consists of an inverter circuit, dc-link capacitor and control scheme [5]. This control scheme is responsible for estimating the current harmonics, maintaining dc-link voltage and generating switching pulses.

In recent years, IT2 FLCs have been attracting great research interests. They are a powerful tool and better able to handle uncertainties than their type-1 in complex processes [6], [7], [8], [9], [10], [31]. IT2 FLCs can outperform conventional T1 FLCs in presence of external disturbances and noises. Because of the additional degree of freedom provided by the footprint of uncertainty (FOU) in their membership functions [11], [12]. Consequently, IT2 FLCs have been applied in various areas especially in control system design. However, fuzzy logic also has its shortcomings; designing IT2 FLCs is more difficult because there are more parameters involved. Lack of systematic procedures, for design and tuning of fuzzy systems, have been considered as a main disadvantage of FLCs [13], and have limited their applications.

There are numerous structures of multi level inverter, and filters as well knew an evolution in it structures from two-level to multi-level. The NPC inverter topology has been the centre of research and development effort for several applications [14]. Current paper invests in advantages of five-level NPC inverter, such as reduced switching losses, smaller output current ripple as compared with that of a conventional type, and total supply voltage is split; only half of the voltage has to be switched, and this also cuts the switching losses in the transistor by half all this will reduce the effort for filtering and isolation in the filter inductor [15].

The application of IT2 FLC in intelligent control has been considered in this paper. Where the performance of the shunt active power filter has been evaluated in term of harmonic mitigation and dc-link capacitor voltage regulation, we have developed IT2 FLC in order to maintain it constant and to generate the compensating reference currents. Numerous measurements and criteria are discussed, for quantifying the errors, we utilized tow widely used performance criteria, which are integral of the absolute value of the error (IAE), and integral of the time multiplied by the absolute value of the error (ITAE). Analyses of the results are presented as a part of this study.

2. Parallel active filter

Figure 1 appears the synoptic of parallel active filter, it contains from an inverter with storage element and an inductive output filter.

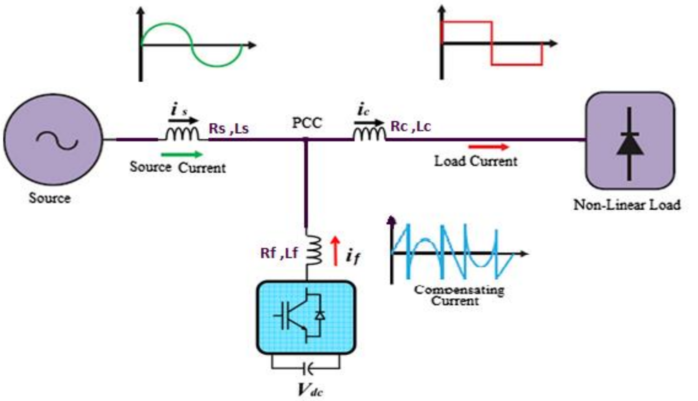

Fig.1. Basic configuration of shunt APF

3. Harmonic reference extraction

3.1 Synchronous reference frame strategy

The performance of an APF depends mainly on the technique selected to generate reference compensating current. The template to generate the reference current must include amplitude and phase information to produce the desired compensating current while keeping the voltage across the DC bus capacitor constant. The chosen technique must operate satisfactorily under both steady state and transient conditions [17]. Several algorithms in time and frequency domain are being used for calculation of reference currents harmonics. Synchronous reference frame (SRF) is one of popular methods harmonic component extraction. In this method, the load current at the point of common coupling (PCC) is measured then has already been transformed from (abc) stationary coordinate to (dq-0) rotating coordinate system transformation [16]. It is done using following figure.

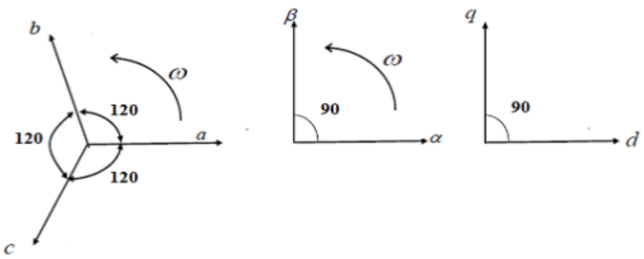

Fig.2. Reference frame transformation

First, identified and transformed into stationary two-phase frame (αβ-0) from the three-phase stationary frame (abc), as per (1).

$$\begin{pmatrix} i_\alpha \\ i_\beta \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & 1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{pmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{pmatrix} \quad (1)$$

After, the two phase current quantities i_α and i_β of stationary (αβ-0) axes are transformed into two-phase rotating synchronous frame (dq-0) using (2).

$$\begin{pmatrix} i_d \\ i_q \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin(\theta) & -\cos(\theta) \\ \cos(\theta) & \sin(\theta) \end{bmatrix} \begin{pmatrix} i_\alpha \\ i_\beta \end{pmatrix} \quad (2)$$

Phase Locked Loop circuit (PLL) is used in order to provide cos (θ) and sin (θ) which represents the synchronous unit vectors for transformation of the supply current source. Equation (2) contains AC component or oscillating value as well as DC component or average value, see (3). *j*

$$\begin{pmatrix} i_d \\ i_q \end{pmatrix} = \begin{pmatrix} \overline{i_d} & \tilde{i}_d \\ \overline{i_q} & \tilde{i}_q \end{pmatrix} \quad (3)$$

To eliminate the AC component which contain harmonic component, low pass filter is used. So that DC component which is output of above equation is harmonic free.

Next, this harmonic free signal in (dq-0) rotating frame is converted back into (abc) stationery frame as shown below.

$$\begin{pmatrix} i_{ah} \\ i_{\beta h} \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin(\theta) & -\cos(\theta) \\ \cos(\theta) & \sin(\theta) \end{bmatrix}^{-1} \begin{pmatrix} \tilde{i}_d \\ \tilde{i}_q \end{pmatrix} \quad (4)$$

Finally, the current from two phase stationary frame (αβ-0) is transformed back into three-phase stationary frame (abc) and the compensation reference currents i_a*, i_b* and i_c* are obtained us peer in (5).

$$\begin{pmatrix} i_a^* \\ i_b^* \\ i_c^* \end{pmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ 1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{pmatrix} i_{ah} \\ i_{\beta h} \end{pmatrix} \quad (5)$$

Figure 3 illustrates the internal structure of SRF. The magnitude of peak reference current $I_{\_max}$ which is the output of FLC is added to the extracted supply current DC component in (dq-0) reference frame. $I_{\_max}$ takes response of the active power demand for harmonics and reactive power compensation.

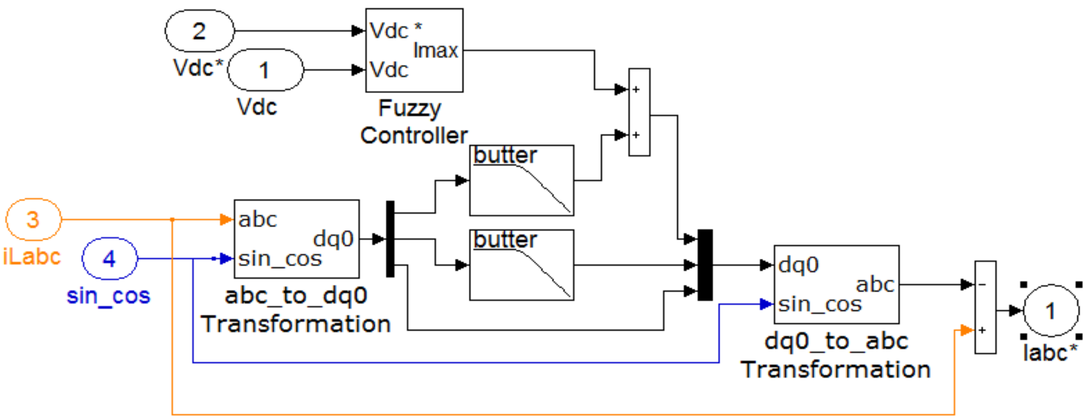

Fig.3. Reference frame transformation

In Figure 4, the SRF is clearly defined in the control strategy circuit. The DC-link voltages Vdc1, Vdc2, Vdc3 and Vdc4 are equals and utilized for the generation of $I_{\_max}$. The peak value of the reference current $I_{\_max}$ is estimated by regulating the DC-bus capacitor voltage of five-level NPC inverter using fuzzy logic controller (FLC).

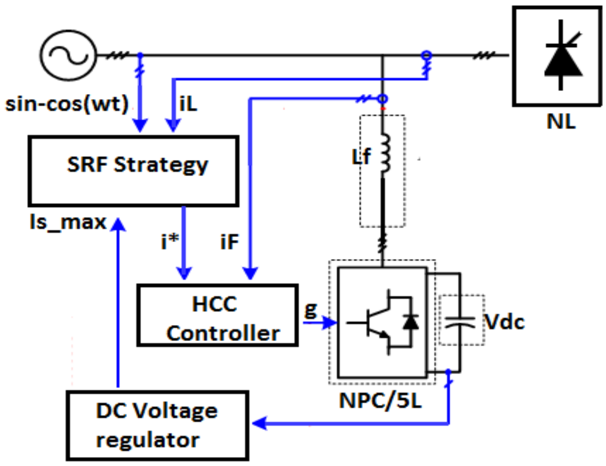

Fig.4. Control strategy circuit diagram

4. NPC Inverter Five Level

4.1 Knowledge model of five-level NPC

Many multilevel inverter topologies have been proposed, and one of the most popular topology is the neutral point clamped (NPC) inverter. In Figure 5 the proposed NPC five-level inverter consists of four (04) series connected capacitors C1, C2, C3 and C4. The dc-link capacitors divide the DC bus voltage into five levels namely +2Vdc, +Vdc, 0, -Vdc and -2Vdc. Each leg of the inverter has (08) bidirectional switches, (06) in series and (02) in parallel plus (02) diodes to get zero voltage. Each switch is composed of a transistor and a diode in antiparallel [18].

Under the balanced condition Vdc1=Vdc2=Vdc3=Vdc4=Vdc/4. For the control strategy shows in Figure 4 the total dc-link capacitor voltage Vdc is the sum of all the four dc-link voltages which has been utilized for the generation of $I_{\_max}$ of reference current.

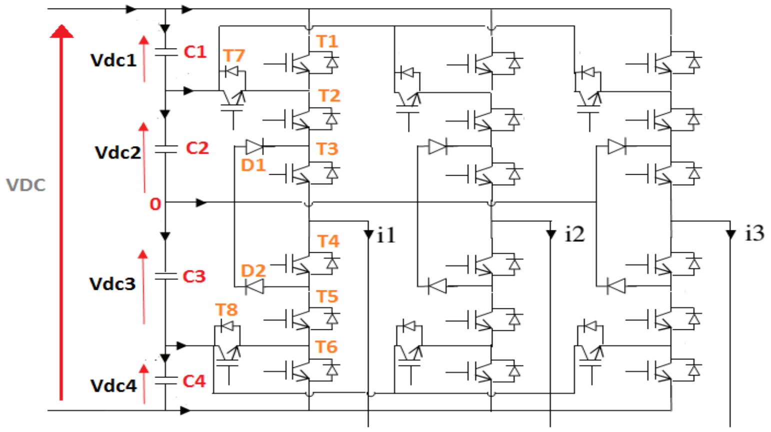

Fig.5. Five level NPC current source inverter

In Table 1, the switching states can be generated using (6).

$$\begin{cases} T_6 = \overline{T}_1 \\ T_4 = \overline{T}_2 \\ T_5 = \overline{T}_3 \\ T_7 = \overline{T}_1.T_2.T_3 \\ T_8 = \overline{T}_6.T_4.T_5 \end{cases} \quad (6)$$

4.2 Hysteresis Current Control Strategy

The hysteresis band current control for APF is used to generate the switching pattern of the inverter. For reason that it is characterized by unconditioned stability, very fast response and high quality of precision [19], the Hysteresis Current Control (HCC) technique plays an essential role in the development of shunt APF.

In Figure 6, the desired currents and real compensating currents are compared to create the errors value e_k. These current errors signals become the inputs to the hysteresis block control in order to drive the inverter in manner to minimize the error which in turn controls all the system.

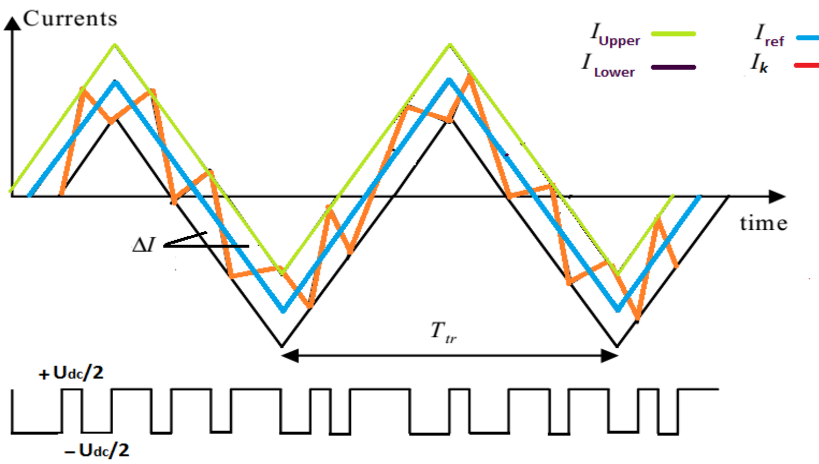

Fig.6. Simplified diagram of hysteresis band current controller

The five-level hysteresis control algorithm is given by (7).

$$\begin{cases} e_k > 2\Delta I \\ \Delta I < e_k < \Delta I \\ -\Delta I < e_k < \Delta I \\ -2\Delta I < e_k < -\Delta I \\ e_k < -2\Delta I \end{cases} \begin{cases} \Rightarrow T1 = 0, T2 = 0, T3 = 0 \\ \Rightarrow T1 = 1, T2 = 0, T3 = 0 \\ \Rightarrow T1 = 0, T2 = 0, T3 = 1 \\ \Rightarrow T1 = 0, T2 = 1, T3 = 1 \\ \Rightarrow T1 = 0, T2 = 0, T3 = 1 \end{cases} \quad (7)$$

Where: ΔI is the width of hysteresis tolerance band. And

$$\begin{cases} e_{k=(a,b,c)} = I_{k\_ref} - I_k \\ \begin{cases} I_{k\_upper} = I_{k\_ref} + \Delta I \\ I_{k\_lower} = I_{k\_ref} - \Delta I \end{cases} \end{cases} \quad (8)$$

5. Basic concepts of type-2 fuzzy sets

The theory of fuzzy sets (FSs) was introduced by Zadeh [20], in 1965. A type-2 fuzzy set denoted **Ã** may be represented via (9).

$$\tilde{A} = \{((x,u), \mu_{\tilde{A}}) | \ \forall x \in X, \forall u \in J_x \subseteq [0,1]\} \quad (9)$$

In which $0 \leq \mu\tilde{A}(x, u) \leq 1$ and x is input variables called the primary variable, has domain X and $u \in [0, 1]$ called the secondary variable, has domain $Jx \subseteq [0, 1]$ at each $x \in X$.

In Figure 7, an example of a T2 FS is shown. A T2 FS is bounded from above and below by two T1 FSs $\underline{\mu}_{\tilde{A}}(x)$ and $\overline{\mu}_{\tilde{A}}(x)$ which are called upper and lower membership function respectively. The area between $\underline{\mu}_{\tilde{A}}(x)$ and $\overline{\mu}_{\tilde{A}}(x)$ is the Footprint Of Uncertainty (FOU).

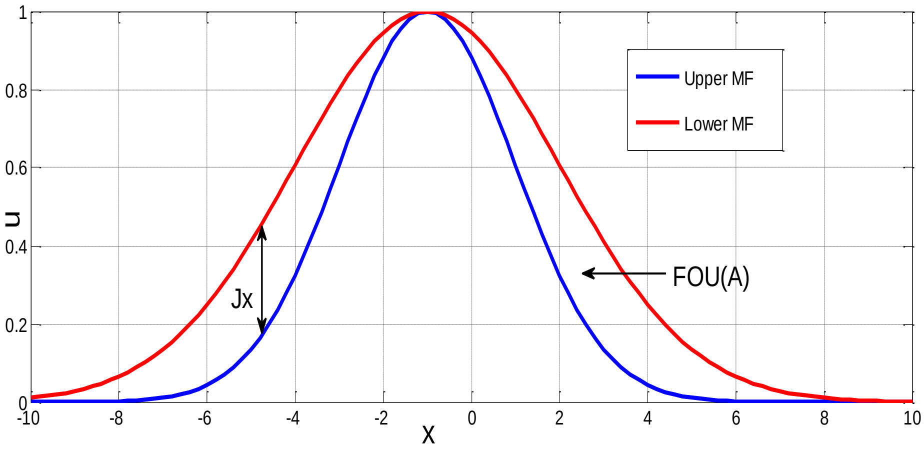

Fig.7. Gaussian type-2 fuzzy membership function

5.1 Interval Type-2 Fuzzy Sets

When all μÃ (x, u) are equal to 1, then **Ã** is an interval T2 FLS. It is defined as [21].

$$\tilde{A} = \int_{x \in X} \int_{\mu(x) \in J_x} 1/(x, \mu(x)) = \int_{x \in X} \left[\int_{\mu(x) \in J_x} 1/\mu(x) \right] / x \ , J_x \subseteq [0,1] \ (10)$$

In (10), ∫∫ denotes union over all admissible x and $\mu(x)$. Note that Jx is an interval set, i.e.

$$J_x = [\underline{\mu}_{\tilde{A}}(x), \overline{\mu}_{\tilde{A}}(x)] \quad (11)$$

Where

$$\underline{\mu}_{\tilde{A}}(x) = \min(J_x), \forall x \in X \quad (12)$$

$$\overline{\mu}_{\tilde{A}}(x) = \max(J_x), \forall x \in X \quad (13)$$

The FOU of **Ã** can also be expressed as [29].

$$\mathrm{FOU}(\tilde{A}) = \bigcup_{\forall x \in X} J_x = \bigcup_{\forall x \in X} \left[\underline{\mu}_{\tilde{A}}(x), \overline{\mu}_{\tilde{A}}(x)\right] \quad (14)$$

Generally, an IT2 FLC includes five basic parts: fuzzifier, rule base, fuzzy inference engine, type reducer, and defuzzifier as shows in Figure 8.

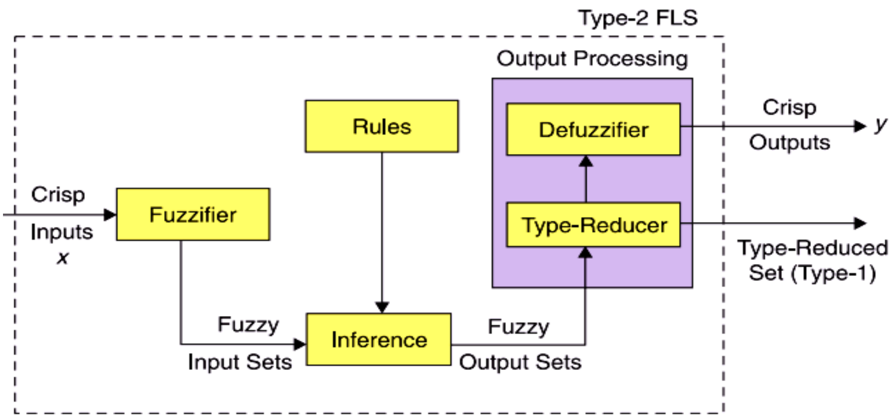

Fig.8. Structure of an IT2 FLS

- **Fuzzifier**

The fuzzifier maps the crisp input vector x =(x1, x2 ... xn)^T to a T2 FS Ãx. It is similar to the procedure performed in a T1 FLS.

- **Rules base**

The general form of the jth rule of a T2 FLS can be written as

$$if\ \mathrm{x}_1\ is\ \tilde{F}_1^j\ and\ \mathrm{x}_2\ is\ \tilde{F}_2^j\ and\ \mathrm{x}_n\ is\ \tilde{F}_n^j\ then\ y = \tilde{G}^j, j = 1,2,\ldots,M \quad (15)$$

Where M is the number of rules, *xi (i=1, 2,…, n)* and y are the input and output of the IT2 FLS respectively . $\tilde{F}_1^j$ presents the T2 FS of input state i of the jth rule and $\tilde{G}^j$ is the output of T2 FS for rule *j*.

- **Inference engine**

In IT2 FLS, the inference engine combines rules and gives a mapping from input IT2 FSs to output IT2 FSs. using performing input and antecedent operations, the firing input sets are defined based on their upper $\overline{f}^{j}(X)$ and lower $\underline{f}^{j}(X)$ MFs as

$$F^{j}(X)=\prod_{i=1}^{n}\mu_{\tilde{F}_1^{j}}(x_i) \quad (16)$$

$$F^{j}(X)=[\underline{f}^{j}(X),\overline{f}^{j}(X)] \quad (17)$$

$$\underline{f}^{j}(X)=\underline{\mu}_{\tilde{F}_1^{j}} * \underline{\mu}_{\tilde{F}_2^{j}} * \ldots\ldots\ldots\ldots * \underline{\mu}_{\tilde{F}_n^{j}} \quad (18)$$

$$\overline{f}^{j}(X)=\overline{\mu}_{\tilde{F}_1^{j}} * \overline{\mu}_{\tilde{F}_2^{j}} * \ldots\ldots\ldots\ldots * \overline{\mu}_{\tilde{F}_n^{j}} \quad (19)$$

- **Type Reducer**

Since the output of the inference engine is a type-2 fuzzy set, a type-reducer is needed before defuzzification to convert type-2 fuzzy sets into type-1. Because it can be computed more easily, center of sets (COS) reduction is usually used. Y_{coc} is an interval set that is determined with its left-end point y_l, and right-end point y_r. Y_{coc} can be expressed as [22].

$$Y_{\cos}=[y_l,y_r]=\int_{y^1\in[y_l^1,y_r^1]}\cdots\int_{y^M\in[y_l^M,y_r^M]}\cdots\int_{f^1\in[\underline{f}^1,\overline{f}^1]}\cdots\int_{f^M\in[\underline{f}^M,\overline{f}^M]}1/\frac{\sum_{i=1}^{M}f^i y^i}{\sum_{i=1}^{M}f^i} \quad (20)$$

- **Defuzzifier**

Karnik and Mendel algorithm presents iterative procedures to compute y_l and y_r in [23]. The defuzzified crisp output from an IT2FLS is the average of y_l and y_r [24].

$$Y_{output}(x)=\left[\frac{y_l+y_r}{2}\right] \quad (21)$$

6. DC Bus Voltage Regulation

6.1 DC voltage control loop

Voltage capacitor is considered as a voltage supply source for active filter and its value must be kept constant to ensure that the performance of the filter is maintained and the voltage fluctuations of the semiconductors do not exceed the limits prescribed. The IT2 FLC is implemented as exposed in Figure 9.

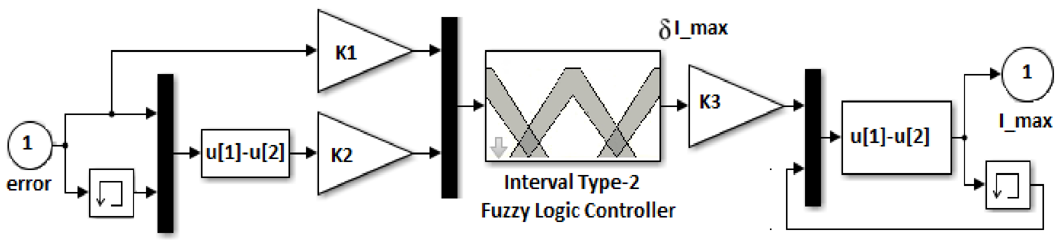

Fig.9. IT2 FLC block diagram

The IT2 FLC does not require a mathematical model of the system, its internal structure needs 2 inputs error e(k) and variation in error Δe(k). The output after a limit is considered as the amplitude of the reference current I_max(k) takes care of the active power demand of load and the losses in the system. The internal structure of IT2 FLC is defined as

$$\begin{cases} e(k) = V_{dc}^{*}(k) - V_{dc}(k) \\ \Delta e(k) = e(k) - e(k-1) \\ I_{\max}(k) = I_{\max}(k-1) + \delta I_{\max}(k) \end{cases} \qquad (22)$$

Seven triangular membership functions are used for the implemented IT2 FLC and seven fuzzy levels or sets are chosen as: NB (negative big), NM (negative medium), NS (negative small), ZE (zero), PS (positive small), PM (positive medium), and PB (positive big) [25], [32] to convert these numerical variables into linguistic variables as in Figure 10. The diagonal rule table is summarized in Table 2

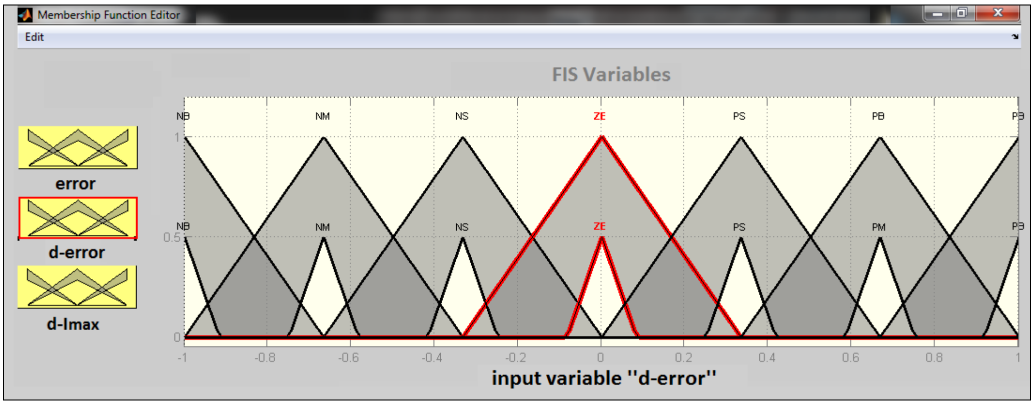

Fig.10. Membership functions for e, Δe & δImax

7. Performance criteria

For evaluating the transient closed-loop response, we can use the criteria performance IAE and IATE given in (23) and (24).

- Integral of the Absolute value of the Error

$$IAE = \int_0^\infty |e(t)| dt \quad (23)$$

- Integral of the Time multiplied by the Absolute value of the Error
-

$$ITAE = \int_0^\infty t|e(t)| dt \quad (24)$$

8. Simulation and discussing results

In recent years type-2 FLCs have become increasingly popular due to their ability to cope with uncertainties. In present study the robustness of the T2 FLC is tested under presence of three sources of uncertainties. The noise of the measurement devices (test B), model uncertainty L_f is introduced with 50% of the nominal value (test C) and there are modeling and measurement uncertainties which are a combination of previous uncertainties (test D) .all results of simulation are compared with ideal system without uncertainties which considered us test A

In order to evaluate the feasibilities of T2 FLC, two commonly performance measuring criteria such as integral of the absolute value of the error (IAE), and integral of the time multiplied by the absolute value of the error (ITAE) are adopted. The values obtained for all tests are show as per in Table 3.

Table 4 contains the system parameters considered for the study. The simulation of shunt APF is carried in MATLAB/SimPower systems environment.

In the simulation tests, the system performance is initially analyzed without uncertainties, during which it is observed that the source current is purely sinusoidal after filtering and the respective THD is 1.16% which is below 5% (IEEE standard 519-1992). In this ideal case, it can be remarked that the dc-link capacitor voltage is well regulated and maintained at a constant value of 600V in shorter time with a very limited fluctuation, see test (A) in Figures 11, 12 and 13. In addition lower values of IAE and ITAE in Table 2 confirm the best performance of the proposed IT2 FLC and shunt APF is able to mitigate the harmonics perfectly once it has chosen a perfect method of control.

The purpose of the second test is to evaluate the robustness level of the proposed approach. It presents the parametric variations or changes of filter inductance with 50%. Indeed, these variations impose an increase of THD; it is 1.65%. Quality of source current waveforms is extremely good. The dc bus voltage remains almost constant within the acceptable limits using

IT2 FLC in spite of the uncertainty while the controller has a small steady state. The simulation results of test (B) in Figures 11, 12 and 13 are clearly showed that shunt APF is succeeded in compensating harmonic currents.

In the third test, a random noise with normal distribution is added, to the measurement values of current filter. We also note slight increase in THD value of source current compared by test (A), it is 1.34% which is strictly within the limits of the standards. No change in regulating and maintaining of dc-link capacitor voltage; IAE and ITAE values are considered lower 2.18 and 0.194 respectively. Good dynamic response of APF has been shown from the simulation results of test (C) in Figures 11, 12 and 13 despite the uncertainty of measurement.

In test (D), the disturbances part applied on the global system is represented by a combination between previous uncertainties. It can be seen that due to the effects of uncertainties, the THD value is amplified; it is 2.11% of fundamental source current which is satisfactory within the limits of the standards. Source current is entirely sinusoidal and the dc-link capacitor voltage is kept constant at 600V. All results are demonstrated in Figures 11, 12 and 13.

To demonstrate the ability of the IT2-FLC and APF performance to compensate harmonics in presence of different disturbances and non-linearity of global system, the THD values of current source under A, B, C and D tests for 3th, 5th, 7th, 9th, 11th, 13th, 15th, 17th and 19th order of harmonics are summarized in Figure 14. Line graphs are clearly illustrates the amount of THD of source current under various source.

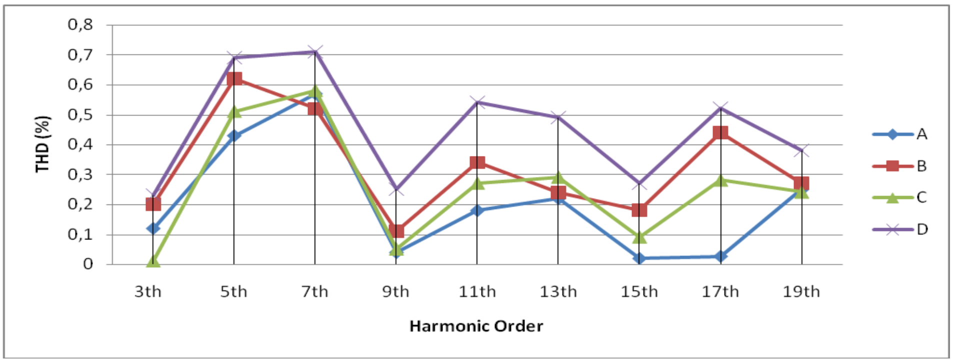

Fig.13. Comparative THD Graphs of source current for A, B, C & D test

9. Comparative analysis of the results

In [26], a new adaptive control technique is described for shunt APF using IT2 FLC based on five Gaussian MFs for representing each linguistic variable. Authors have chosen a comparison method between T1 and T2 FLC to analyzed and studied for different voltage of balanced and unbalanced conditions. Compared with our approach which requires seven Triangular MFs and 49 rules base the computing time can be considerably reduced.

Dhanavath Suresh and Saijan Pal Singh in [27] proposed T2-FLC to improve the power quality in Shunt APF. Authors used p-q theory to extract the compensating current based three-level NPC inverter. However, this control strategy is not succeeded in compensating harmonic currents, notches are observed in the source current. Compared with present study, SRF strategy is used, and the APF based on five-level NPC inverter reduced more the THD and ensure the stability and the robustness of the control structure.

Using three Gaussian MFs for T2-FLC in [28] to enhance the grid power quality in presence of modeling uncertainties are inadequate compared with our approach. Because the number of linguistic variables is directly related to the accuracy of approximating functions and plays an important role for approximating the nonlinear input output mapping. As the number of linguistic variables increases the output of the FLC becomes a linear function of the input.

Conclusion

In this paper, shunt active power filter based five-level NPC inverter was studied and simulated in the synchronous reference frame. Is have been analyzed for different uncertainties and non-linearity conditions. The use of the IT2-FLC provides more flexibility and makes the scheme more robust and less susceptible to disturbances parametric and measurement. The performance of the proposed controller has been evaluated in terms the harmonic distortion of the source current waveforms and variations in the filter inductance. The exhaustive simulation results are successfully validating the controller dynamic performance and the harmonic distortion achieved with the proposed controller was well below the limit imposed by the IEEE-519 standards. Compared with other authors' results, present study proved the feasibility and effectiveness of shunt APF which can be considered as a reliable harmonic isolator for its quick response and good quality of filtering.

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Appendix

Table.1. Switching states 5L NPC inverter

Output level Voltage	Switching States for First Leg		
	T1	T2	T3
2Vdc	1	1	1
Vdc	0	1	1
0	0	0	1
-Vdc	1	0	0
-2Vdc	0	0	0

Table 2. Fuzzy rule table

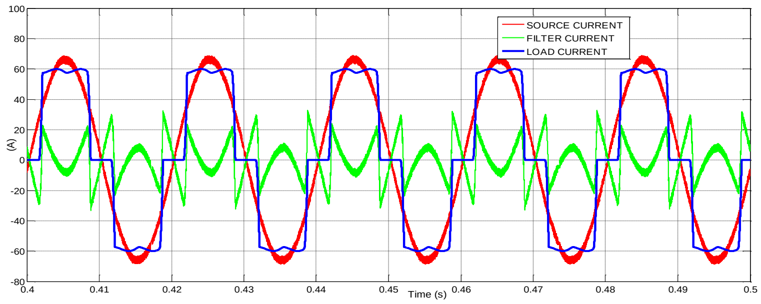
e \ Δe	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	NM	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

Table.3. Performance criteria values of IT2 FLC

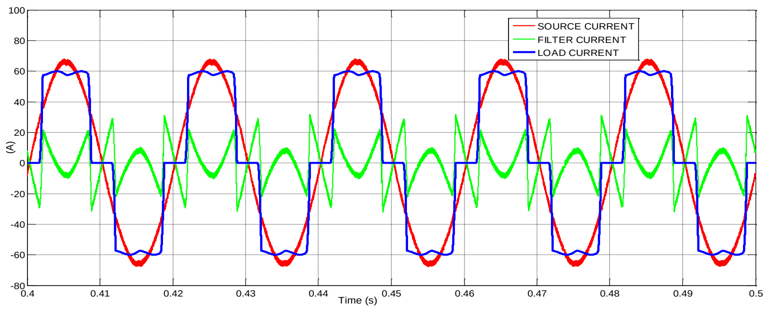
	Sys without Uncertainty -A-	Modeling Uncertainty -B-	Measurement Uncertainty -C-	Modeling & Measurement Uncertainty -D-
IAE	2,17	2,25	2,18	2,24
ITAE	0,193	0,2	0,194	0,21

Table.4. System parameters

Network	Non Linear Load	Shunt APF	IT2 FLC & HCC
Vs=220V F=50Hz	R_l=5Ω L_l=8.10^{-3}H	C=2200.10^{-6}F L_f=1.10^{-3}H	Vdc*=600V
			seven T2-Triangular MFs Matrix (7x7) rules base
			ΔI=0.1A



-A-



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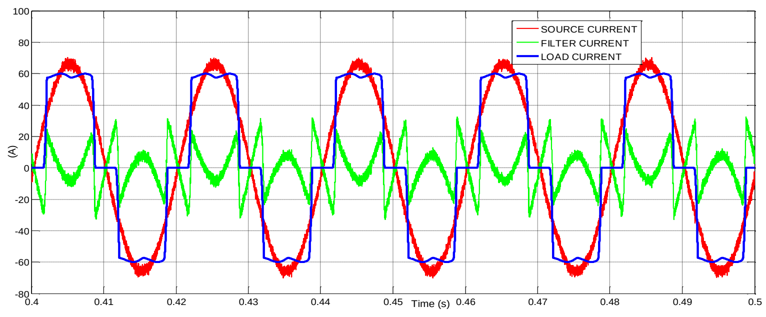

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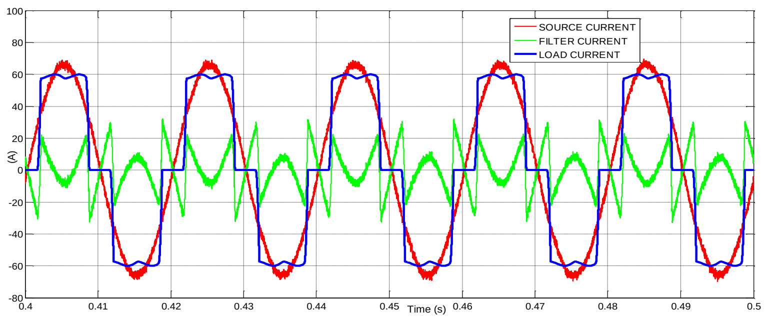
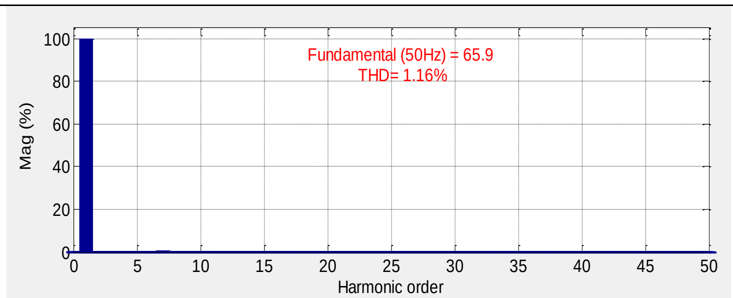


-D-

Fig.11. Load, filter and source current phase (a) for A, B, C & D test



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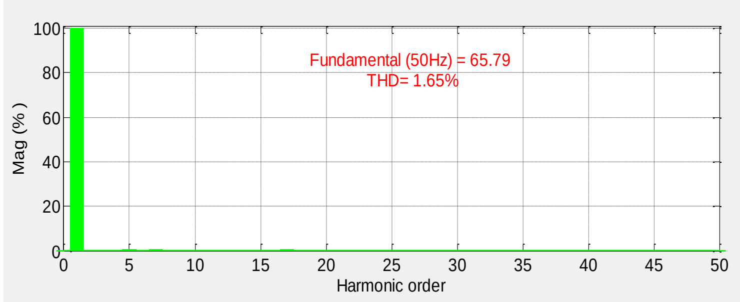
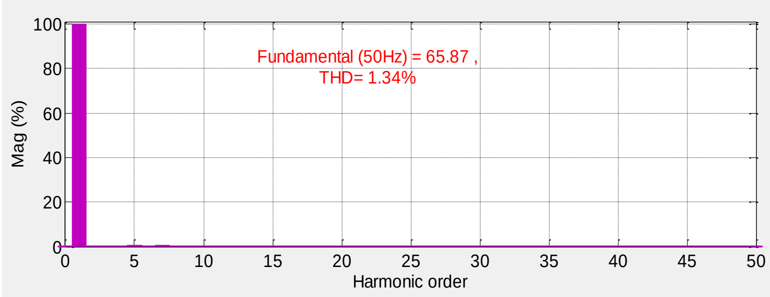
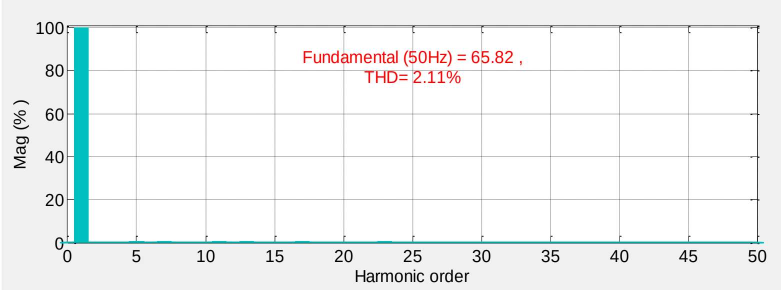


-B-

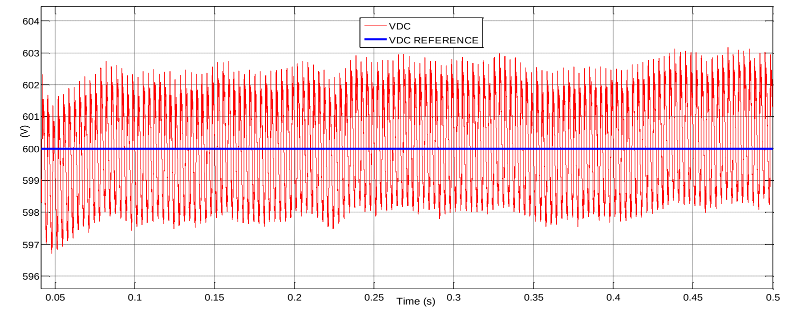


-C-

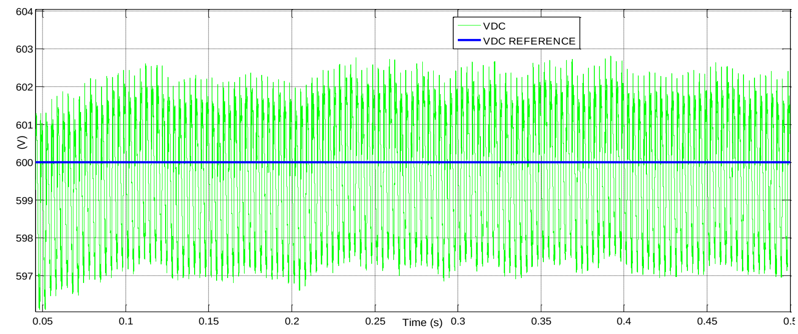


-D-

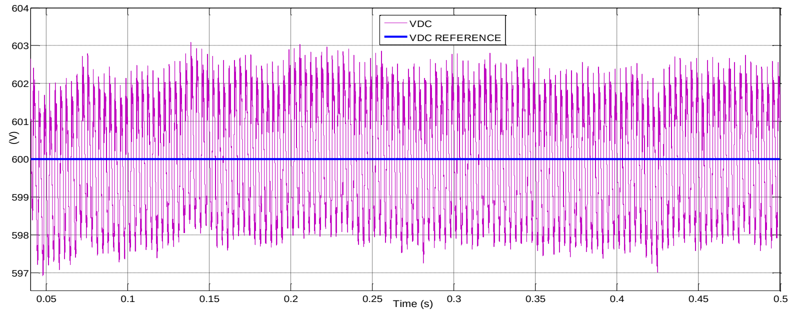
Fig.12. Harmonic analyze of current source phase (a) for A, B, C & D test



-A-



-B-



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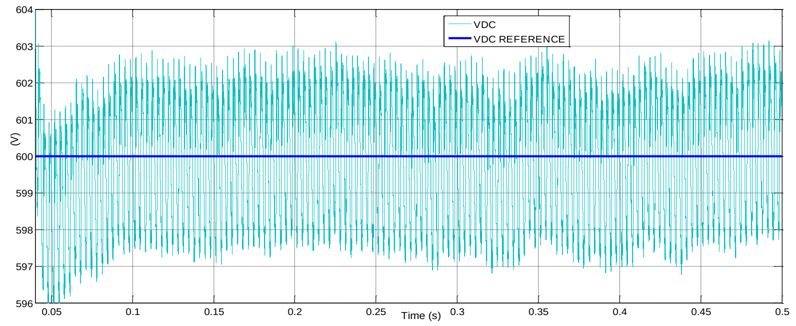

-D-

Fig.13. DC-link Capacitor voltages for A, B, C, D test