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Performance Evaluation of Dynamic Voltage Restorer Under Asymmetrical Faults and Dynamic Unbalanced Loads

Raed Najim Ibrahim[1*], Mohammed Y. Suliman[1], Mohamed Salem Mohamed Othman[2]

[1] Department of Electrical Engineering Techniques, Engineering Technical College of Mosul, Northern Technical University, Mosul 41001, Iraq
[2] School of Electrical and Electronic Engineering, Universiti Sains Malaysia, Nibong Tebal 14300, Malaysia

Corresponding Author Email: raed.nagim@ntu.edu.iq

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ABSTRACT

Asymmetrical faults and time-varying phase-voltage disturbances cause voltage unbalance in three-phase distribution systems. This paper evaluates a dynamic voltage restorer (DVR) using conventional discrete direct-quadrature proportional-integral (dq-PI) load-voltage feedback in MATLAB/Simulink. The tests cover single line-to-ground (SLG), line-to-line (LL), and double line-to-ground (LLG) faults, programmed single-phase source-voltage modulation, and unbalanced load switching. Voltage-unbalance factor (VUF) and root-mean-square (RMS) phase-voltage error are assessed in per unit (p.u.). For the LLG fault, phase-A and phase-B RMS values increase from 0.126 and 0.118 to 0.983 and 0.981 p.u. with compensation. In the switched-load test, phase-RMS deviations reach about 12%, consistent with an unregulated zero-sequence component; the cause was not isolated. The low VUF therefore indicates negative-sequence reduction rather than complete restoration of phase magnitudes. The results apply to the investigated simulation model.

1. INTRODUCTION

Three-phase distribution networks increasingly supply sensitive power-electronic loads, making voltage quality at the load terminals important for reliable operation [1, 2]. Voltage sag and swell are well-known disturbances, while voltage unbalance arises when unequal phase magnitudes or angles introduce negative-sequence components. Unbalance is associated with asymmetrical faults, unequal single-phase loading, feeder-impedance asymmetry, and uneven distributed generation [2, 3], and can produce negative-sequence currents and associated equipment stress.

A dynamic voltage restorer (DVR) is a series compensator that injects a controlled voltage to restore the load voltage [1, 4]. Previous DVR studies have mainly advanced controller design or gain selection. Rahman and Dagnew [5] examined voltage-sag compensation using a direct-converter-based DVR with error-signal modulation. Hassanein et al. [6] applied a DVR in an off-grid hybrid renewable-energy system. Rawa et al. [7] used the gorilla troops algorithm to tune proportional-integral (PI) control; Mahmoud et al. [8] applied Harris hawks optimisation to DVR controllers in a low-voltage smart distribution system; Salman et al. [9] compared particle-swarm optimisation with trial-and-error PI tuning; Setty et al. [10] employed hybrid PI-fuzzy control for sag and swell in a photovoltaic (PV)-based network; and Abdelaal et al. [4] examined sliding-mode DVR control for voltage-sag compensation.

These studies address voltage-sag compensation [5], parameter optimisation in diverse DVR operating conditions [7-9], and hybrid control of sag and swell [10]. By contrast, this work quantifies fundamental negative-sequence reduction using voltage-unbalance factor (VUF) under three asymmetrical faults, programmed single-phase source-voltage modulation, and switched phase-dependent loads, while retaining a conventional discrete direct-quadrature proportional-integral (dq-PI) controller. The experiments report regulation accuracy and its limits, rather than a new controller or a cross-controller benchmark.

Because both DVR voltage compensation and some unbalance cases have been studied previously, this paper does not claim a new control algorithm, transformation, modulation technique, or fault category. The investigated controller uses direct–quadrature (dq) coordinates in a synchronous reference frame (SRF) with load-voltage feedback.

The main contributions of this study are as follows:

1. Quantitative evaluation of a conventional discrete dq-PI-controlled DVR using load-voltage feedback during three asymmetrical faults, programmed single-phase source-voltage modulation, and unbalanced load switching.
2. Consistent assessment of the VUF and mean root-mean-square (RMS) phase-voltage error across the three faults, two source-modulation windows, and a distinct switched-load test.
3. Disclosure of the model, controller gains, fault settings, and two distinct time-varying operating tests.

2. CONSTRUCTION OF THE DYNAMIC VOLTAGE RESTORER

The DVR connects in series with the load bus and uses a voltage-source inverter (VSI), filter, injection transformer, and direct-current (DC) supply to regulate load voltage [1, 11, 12]. This configuration is shown in Figure 1.

2.1 Voltage source inverter

The VSI synthesises phase-selective compensating voltages using pulse-width modulation (PWM) [1, 13]. Independent converter-leg switching supports unequal phase-voltage injection [13, 14].

2.2 Injection transformer

The injection transformer transfers the inverter voltage to the feeder and provides galvanic isolation [1, 11, 15]. Its series-voltage capability depends on winding settings, leakage impedance, and saturation margins [16]; the implemented model parameters appear in Section 7.

2.3 Passive filters

An inductor-capacitor (LC) output filter attenuates inverter switching components before series injection [1, 13].

2.4 Energy storage unit

The DC-link supply provides the active energy required for voltage injection [9, 17]. Energy storage or renewable sources may be used [17]; the simulated link is an ideal 200 V DC source and requires a stable voltage for PWM control [1].

2.5 Unbalanced loads

Unequal phase loading, feeder impedance and distributed generation can produce negative-sequence voltage and current components [1, 3]. Their effects include equipment heating and additional losses [1, 2]. The measurements below separate voltage-magnitude error from the negative-sequence VUF [2, 3].

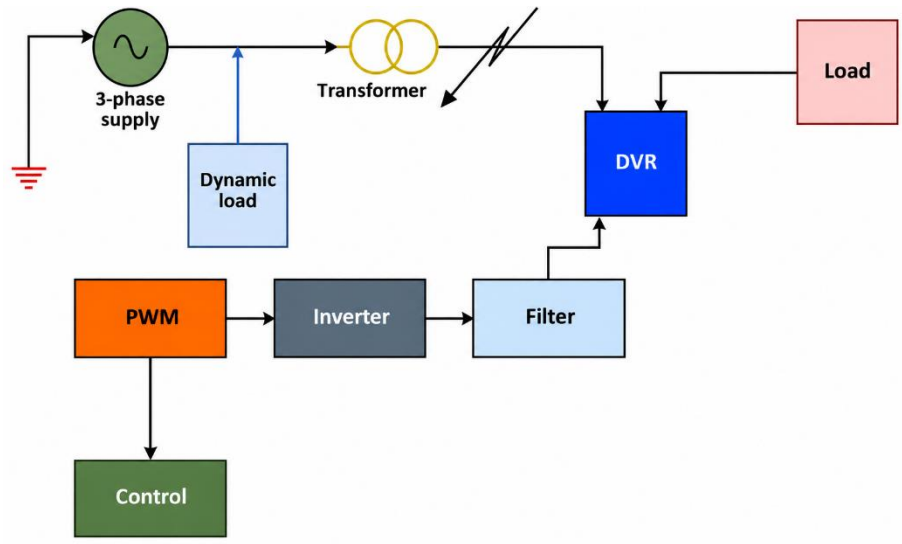


Figure 1. Single-line diagram of the dynamic voltage restorer (DVR) connected in series with the feeder

3. OPERATING PRINCIPLE OF THE DYNAMIC VOLTAGE RESTORER

The investigated DVR regulates the measured three-phase load voltage through synchronous-reference-frame feedback. The load-voltage errors drive discrete PI control commands that actuate the PWM inverter, filter, and series injection transformer; the source, injected, and load voltages satisfy Eq. (7) with consistent terminal polarity.

3.1 Operating modes of the dynamic voltage restorer

3.1.1 Standby condition

During nominal supply conditions, the measured load voltage remains close to the balanced reference; the load-voltage errors and series-injection commands are small, and the controller continues to regulate. No bypass switch or protection logic is included in the simulated model; the DVR remains in series operation throughout.

3.1.2 Injection mode

When a disturbance occurs, the measured load-voltage error produces d- and q-axis controller commands. Following the inverse transformations, the PWM inverter, output filter, and series transformer synthesise the compensating voltage in accordance with the series-voltage relationship in Eq. (7).

The documented control path processes load-voltage feedback continuously; it does not establish a separate, threshold-triggered fault detector. Following fault clearance, the controller remains in closed-loop operation while the measured inverter-side voltage decreases; no bypass switch or protection logic is included in the model.

4. COMPENSATION STRATEGIES

The tested compensation strategy regulates the measured load voltage to a 1 p.u. d-axis reference with q-axis reference zero using discrete closed-loop feedback; no separate pre-sag or in-phase look-up strategy is implemented. The required

injected voltage depends on disturbance magnitude and phase, and thereby affects DC-link energy and converter rating [2, 9, 18].

5. CONVENTIONAL SYNCHRONOUS-FRAME CONTROL

The load-voltage signal $v_{abc} = [v_a, v_b, v_c]^T$ is measured at BUS 2, the load bus immediately downstream of the series injection stage. The phase-to-ground voltage is expressed in per unit (p.u.) using a nominal line-to-line (LL) RMS voltage V_{LL} = 400 V, corresponding to 326.6 V peak phase-to-ground. The Simulink abc-to-dq0 block provides the Clarke–Park transformation, whose stationary-frame components are defined in Eq. (1):

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{1}$$

A discrete virtual phase-locked loop (PLL) supplies the electrical angle θ = ωt. With the rotating frame aligned 90° behind the phase-A axis at θ = 0, Eq. (2) converts the stationary-frame voltages into d- and q-axis components. For a balanced positive-sequence nominal voltage under this sine-reference convention, v_d = 1 p.u. and v_q = 0; the zero-sequence component is not regulated.

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \sin\theta & -\cos\theta \\ \cos\theta & \sin\theta \end{bmatrix}\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \tag{2}$$

The controller uses $v_{d,ref}$ = 1 p.u. and $v_{q,ref}$ = 0. The measured components are subtracted from these references to form the two feedback errors:

$$e_d = v_{d,\mathrm{ref}} - v_d, \quad e_q = v_{q,\mathrm{ref}} - v_q \tag{3}$$

The errors are processed by conventional PI controllers. Their outputs u_d and u_q are modulation commands and not directly measured series-injected voltages:

$$\begin{aligned} u_d(t) &= K_{p,d}e_d(t) + K_{i,d}\int_0^t e_d(\tau)\,d\tau, \\ u_q(t) &= K_{p,q}e_q(t) + K_{i,q}\int_0^t e_q(\tau)\,d\tau. \end{aligned} \tag{4}$$

The empirical gains are $K_{p,d}$ = 40, $K_{i,d}$ = 154, $K_{p,q}$ = 25, and $K_{i,q}$ = 260 (Table 1). The inverse Park transformation uses the same PLL angle and the same reference-frame convention:

$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \begin{bmatrix} \sin\theta & \cos\theta \\ -\cos\theta & \sin\theta \end{bmatrix}\begin{bmatrix} u_d \\ u_q \end{bmatrix} \tag{5}$$

The inverse Clarke transformation with zero commanded zero-sequence component (u_0 = 0) then generates the three-phase commands:

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix}, \quad u_0 = 0 \tag{6}$$

Assuming consistent voltage polarity and neglecting intervening series drops, the source, load, and actual injected phase voltages satisfy:

$$\mathrm{v}_{\mathrm{load},abc} = \mathrm{v}_{\mathrm{source},abc} + \mathrm{v}_{\mathrm{inj},abc} \tag{7}$$

The PI outputs u_d and u_q undergo Eqs. (5) and (6), followed by a unity-gain block before the PWM reference. Each unit modulation command corresponds to an ideal inverter fundamental phase voltage of 100 V peak (70.7 V RMS) with the 200 V DC link; the physical series-injected voltage also depends on the filter and transformer.

The three-phase commands enter the synchronised two-level PWM generator without additional reference normalisation. The PWM block operates in synchronised mode at switching ratio 2225 with a 20 µs sample time. At 50 Hz this ratio gives a nominal carrier of 111.25 kHz, exceeding the 50 kHz update rate; the carrier cycle is not temporally resolved, so the reported results concern fundamental load-voltage regulation rather than resolved switching harmonics.

Table 1. System parameters of the investigated dynamic voltage restorer (DVR)-based distribution system

Parameter	Value
AC Source and Network	
Grid line voltage (rms, L–L)	11 kV
System frequency	50 Hz
Step-down transformer rating	1 MVA
Transformer voltage ratio	11 kV/400 V
Transformer connection	Dyn (Δ-Yg)
Load-bus (distribution) voltage	400 V
Load	
Load configuration	Three-phase, Y-grounded, parallel RLC
Active power, P	1.5 kW
Inductive reactive power, Q_L	500 var
Capacitive reactive power, Q_C	0 var
DVR Power Circuit	
Converter topology	Three-phase two-level Voltage Source Inverter (VSI) (6 IGBTs)
DC-link voltage, V_{dc}	200 V
Output filter inductance, L_f	6 mH
Output filter capacitance, C_f	20 µF
Series injection transformer	Three-phase linear, 1.5 kVA, 1:10 (Table 2)
Control, Modulation and Solver	

Controller type	SRF-based dq PI controller
PI gains, d-axis (K_p/K_i)	40/154
PI gains, q-axis (K_p/K_i)	25/260
Modulation technique	Sinusoidal PWM (SPWM)
PWM switching ratio (carrier/fundamental)	2225 (dimensionless)
Fixed-step sample time, Ts	2×10^{-5} s
Simulation environment	MATLAB/Simulink

Note: VSI = voltage-source inverter; IGBT = insulated-gate bipolar transistor; SRF = synchronous reference frame; SPWM = sinusoidal pulse-width modulation; PI = proportional–integral; PLL = phase-locked loop; dq = direct–quadrature; RMS = root-mean-square; p.u. = per unit.

6. DISCRETE PROPORTIONAL-INTEGRAL GAIN SELECTION

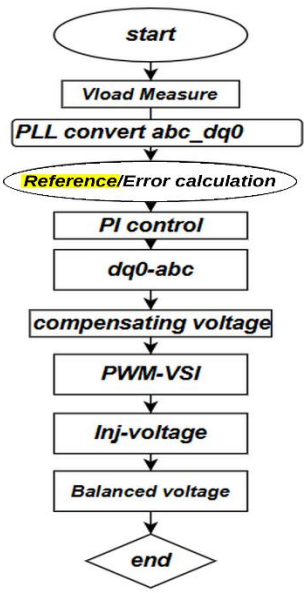


Figure 2. Control scheme of the investigated conventional dynamic voltage restorer (DVR)

The DVR control scheme is shown in Figure 2. Two conventional discrete proportional–integral controllers regulate the synchronous-frame load-voltage errors according to Eq. (4), using the gains listed in Table 1. The resulting u_d and u_q commands are transformed to three-phase PWM references through Eqs. (5) and (6).

We selected the PI gains by manual iterative tuning in MATLAB/Simulink: $K_{p,d} = 40$, $K_{i,d} = 154$, $K_{p,q} = 25$, and $K_{i,q} = 260$ (Table 1). The d- and q-axis gains were tuned separately, and no analytical justification for the difference between them is claimed. Both discrete PI blocks use a 20 µs sample time and forward-Euler integration, zero initial output, and output limits of ±1.1 relative to a PWM carrier range of ±1. These limits permit mild over-modulation under severe disturbances. No separate anti-windup scheme is claimed. Poles, gain and phase margins, and settling time were not computed; no analytical stability proof is claimed.

7. INVESTIGATED SYSTEM MODEL

Design check. Figure 3 shows an 11/0.4 kV feeder with a 1 MVA upstream transformer and a 1.5 kW/500 var test load, with an apparent power of approximately 1.581 kVA (0.158% of the transformer rating). The DVR is supplied by an ideal 200 V DC source and uses a linear series injection transformer with nominal model settings of 10 V and 100 V RMS (1:10) and 1.5 kVA.

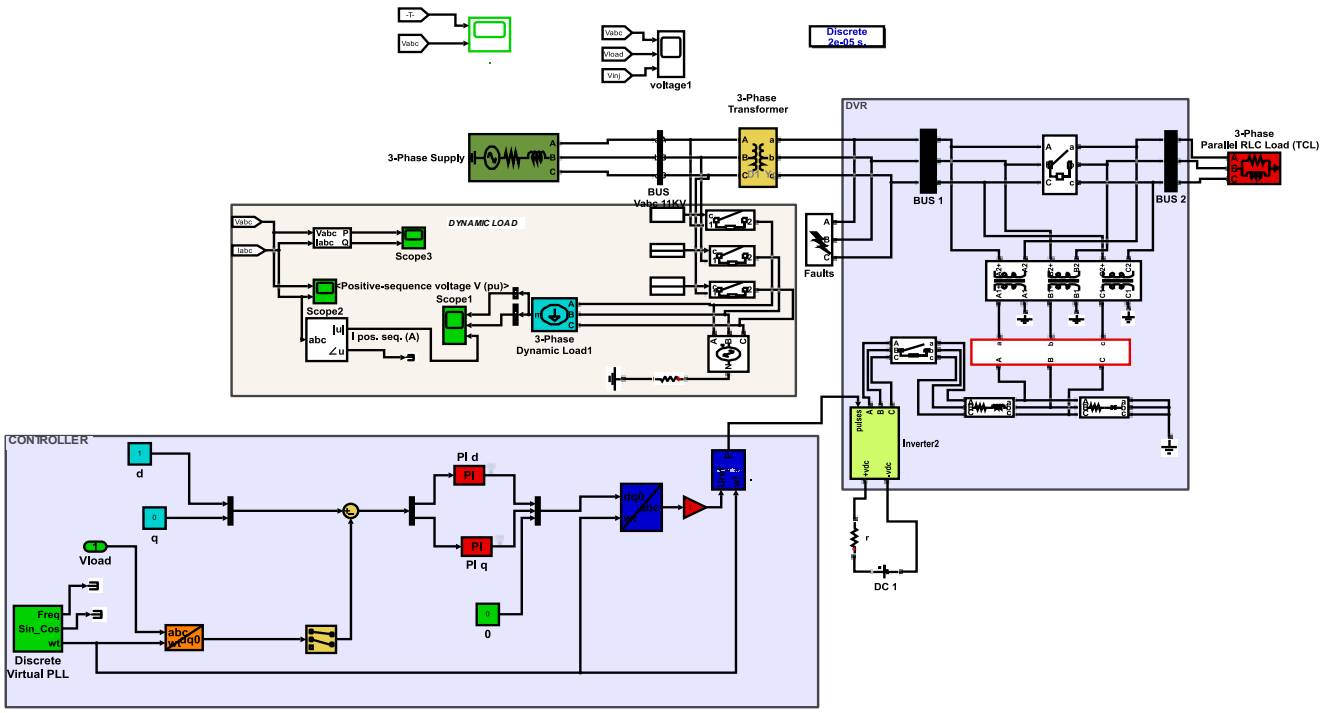


Figure 3. MATLAB/Simulink model of the investigated dynamic voltage restorer (DVR)-based distribution system

Table 2. Model settings of the dynamic voltage restorer (DVR) series injection transformer used in the simulation

Parameter	Value
Configuration	Three-phase linear transformer (12-terminal), series
Nominal power (model setting)	1.5 kVA
Nominal frequency (model setting)	50 Hz
Primary voltage (V_1, RMS; nominal model setting)	10 V
Secondary voltage (V_2, RMS; nominal model setting)	100 V
Turns ratio (N_1:N_2)	1:10
Primary resistance, R_1	1×10^{-5} pu
Primary leakage reactance, X_1	3×10^{-4} pu
Secondary resistance, R_2	1×10^{-5} pu
Secondary leakage reactance, X_2	3×10^{-4} pu
Magnetizing resistance, R_m	200 pu
Magnetizing reactance, X_m	200 pu

Note: p.u. means per unit; RMS means root-mean-square. All winding voltages and apparent power are nominal model settings, not verified hardware ratings.

During the LLG fault, the inverter-side RMS phase voltages over 0.10-0.20 s were 23.2390, 21.5291 and 1.5360 V, corresponding through the 1:10 ratio to approximately 232, 215 and 15 V on the series side (an ideal-ratio estimate, not a direct measurement). The first two exceed the nominal model settings. For an ideal two-level inverter with sinusoidal PWM at unity modulation index, the 200 V DC link gives a theoretical fundamental phase-voltage limit of approximately 70.7 V RMS. The transformer is modelled as linear with specified winding resistance, leakage and magnetising parameters, but without saturation, thermal or winding-current limits; the results therefore describe the simulation model and do not establish that the listed settings are adequate for a physical implementation.

Figure 3 shows the 200 V DC source, two-level VSI, output filter and series injection transformer. The BUS 2 load-voltage measurement supplies the conventional discrete dq–PI feedback loop described in Sections 5 and 6; the transformer model settings are listed in Table 2.

The BUS 2 load-voltage feedback uses the PLL, synchronous-frame transformations, and discrete PI controllers of Sections 5 and 6. Section 8.4 documents the source-modulation and switched-load configurations separately.

8. RESULTS AND DISCUSSION

The results are interpreted through the conventional feedback structure and fixed controller gains (Sections 5 and 6): the asymmetrical fault cases appear in Sections 8.1-8.3, the source-voltage and switched-load tests in Section 8.4, and the measured controller response and regulation limits in Section 8.5. All three asymmetrical faults started at 0.05 s and were cleared at 0.25 s (duration 0.20 s), with fault resistance 0.003 Ω. They comprised a single line-to-ground (SLG) fault on phase A, an LL fault on phases A and B, and a double LLG fault on phases A and B and ground. Grounding resistance was 0.001 Ω for SLG and LLG and did not apply to the ungrounded LL fault. Source-side RMS voltages were evaluated over 0.10–0.20 s relative to the nominal 1 p.u. base; the corresponding voltage drops were 86.5% (phase A, SLG), 41.8% and 58.2% (phases A and B, LL), and 87.4%, 88.2%, and 6.4% (phases A, B, and C, LLG).

Voltage unbalance was quantified using the VUF computed from the fundamental positive- and negative-sequence phase-voltage phasors:

$$\mathrm{VUF} = \frac{|V_2|}{|V_1|} \times 100\% \tag{8}$$

where, $V_1 = (V_a + aV_\beta + a^2V_c)/3$ and $V_2 = (V_a + a^2V_\beta + aV_c)/3$, where a = exp(j2π/3). "Before" values are taken from BUS 1 in the same simulation run; "after" values are measured at BUS 2 downstream of series injection.

8.1 Single line-to-ground fault

The SLG fault reduces one phase while the other two remain unchanged, creating supply-side voltage unbalance. Figure 4(a) shows the uncompensated condition, in which the load voltage follows the disturbed supply and remains unbalanced. In Figure 4(b), the DVR injects voltage only into the disturbed phase during the fault interval; the healthy phases remain unaffected, and the disturbed phase is restored toward the healthy-phase magnitude. Over 0.10–0.20 s, Table 3 reports a source-side VUF of 53.1844%, compared with 0.4426% at the compensated load; the mean post-compensation RMS voltage error was 0.8983%.

Table 3. Voltage-unbalance factor (VUF) and root-mean-square (RMS) voltage errors for single line-to-ground (SLG), line-to-line (LL), and double line-to-ground (LLG) faults and programmed single-phase source-voltage modulation with a dynamic voltage restorer (DVR)

Operating Condition	VUF Before (%)	VUF after (%)	Mean Voltage Error after (%)
SLG fault	53.1844	0.4426	0.8983
LL fault	97.3796	0.5919	0.9921
LLG fault	93.3615	0.3866	1.2517
Source modulation – rise	14.0818	0.1473	0.1541
Source modulation – drop	19.5932	0.1674	0.1522

Note: "Before" denotes source-side phase voltages measured at BUS 1 in the same simulation run; "after" denotes load-side voltages measured at BUS 2. VUF uses the 50 Hz fundamental positive- and negative-sequence phasors. Mean voltage error after compensation is the average absolute departure of the three-phase root-mean-square (RMS) values from 1 per unit (p.u.). The evaluation window is 0.10–0.20 s for faults, 0.40–0.50 s for the source-modulation rise, and 0.90–1.00 s for the drop. Voltages are logged on a 326.6 V peak phase-to-ground base: RMS in p.u. equals √2 times the RMS of the plotted per-unit waveform (1 p.u. RMS equals 230.9 V RMS phase-to-ground).

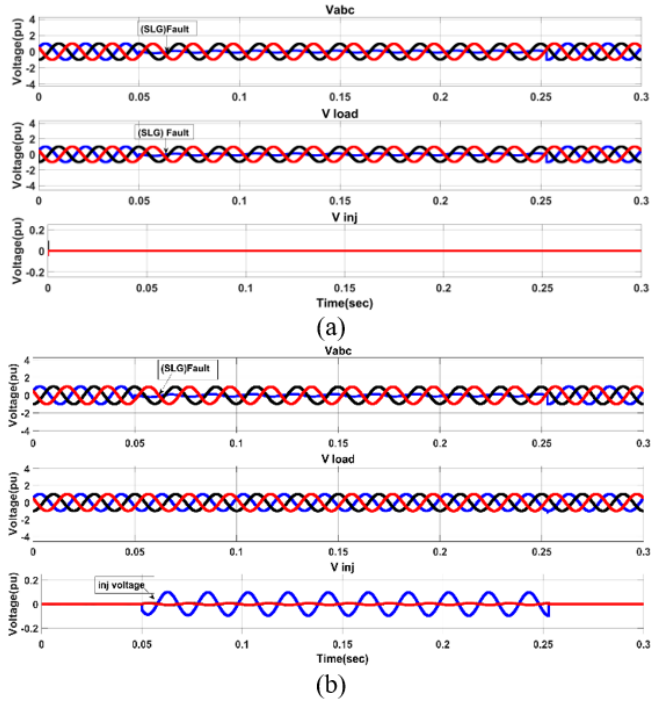


Figure 4. Voltage waveforms during a single line-to-ground (SLG) fault: (a) without dynamic voltage restorer (DVR) compensation; (b) with DVR compensation

8.2 Line-to-line fault

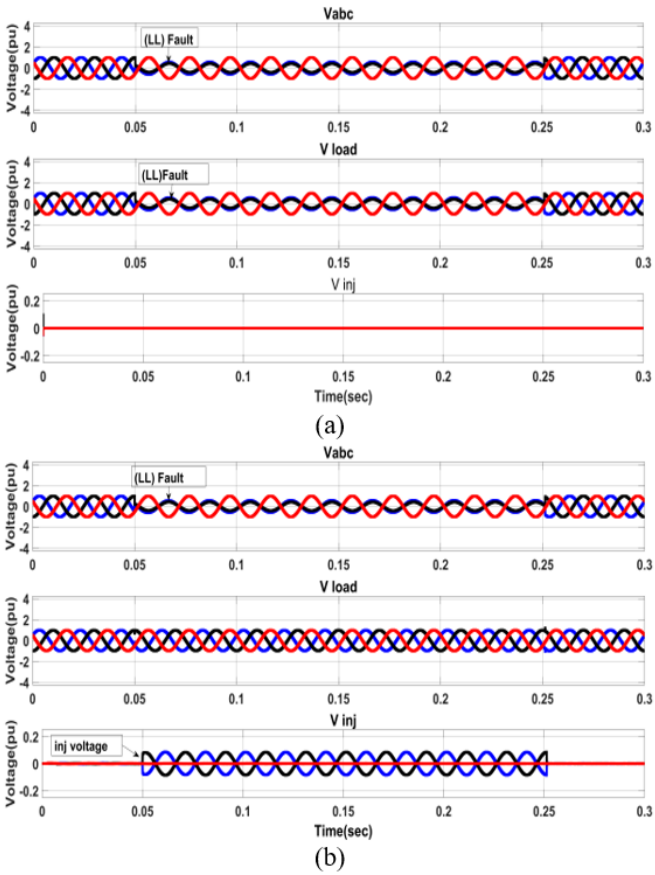


Figure 5. Voltage waveforms during a line-to-line (LL) fault: (a) without dynamic voltage restorer (DVR) compensation; (b) with DVR compensation

The LL fault disturbs two phases, producing an asymmetric load-side voltage when no compensation is applied. Figure 5(a) shows the reduction of the two affected phases and the resulting load-side unbalance. Figure 5(b) shows the DVR injecting the required series voltage into the two disturbed phases during the fault interval, restoring the load voltage toward a balanced three-phase waveform. Table 3 gives a source-side VUF of 97.3796% and a compensated load-side value of 0.5919%; the mean post-compensation RMS voltage error was 0.9921%.

8.3 Double line-to-ground fault

The LLG fault strongly depresses phases A and B, while phase C is less affected. Figure 6(a) shows the uncompensated condition, with the load voltage following the severe two-phase depression. Figure 6(b) shows DVR compensation during the fault. Over 0.10–0.20 s, phase-A and phase-B RMS voltages improve from 0.126 and 0.118 to 0.983 and 0.981 p.u., respectively, while phase C reaches 1.002 p.u. Table 3 reports a reduction in the VUF from 93.3615% to 0.3866%, with a mean post-compensation RMS voltage error of 1.2517%. The "V_{inj}" trace in Figure 6(b), approximately 0.1 p.u. peak, is measured on the inverter side of the 1:10 transformer; it is not a direct measurement of the line-side injected voltage.

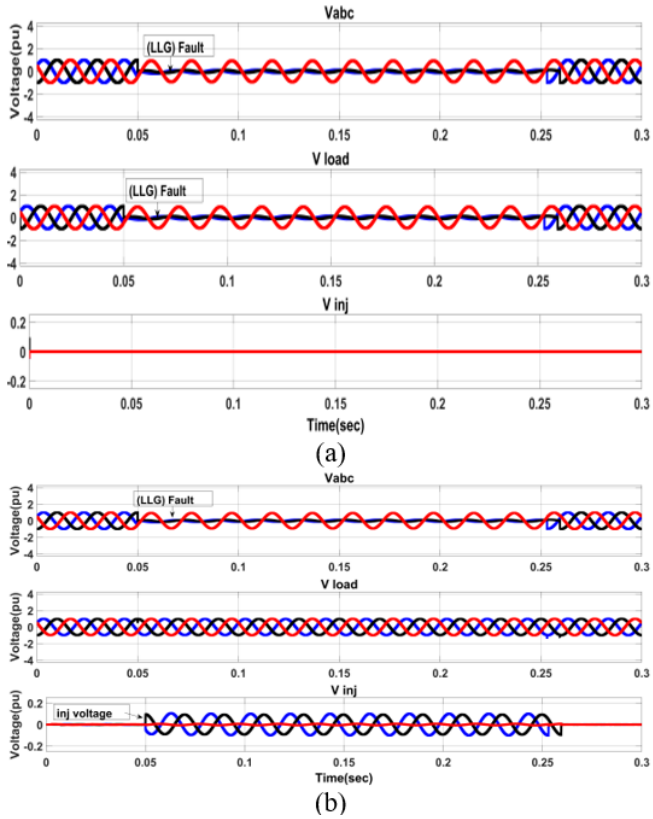


Figure 6. Voltage waveforms during a double line-to-ground (LLG) fault: (a) without dynamic voltage restorer (DVR) compensation; (b) with DVR compensation

Note: The V_{inj} subplot displays inverter-side phase-to-ground voltage (p.u. on the 326.6 V peak phase-to-ground base, equivalent to 400 V line-to-line RMS), not the physical line-side series-injected voltage. Here, p.u. denotes per unit and RMS denotes root-mean-square.

8.4 Time-varying source and switched-load tests

Figure 7(a) shows the uncompensated response to

programmed single-phase source-voltage modulation, while Figure 7(b) identifies the source-side phase voltages at the 11 kV bus and at BUS 1, each on its own per-unit base. The programmed 11 kV, 50 Hz source is connected to phase A through a breaker, with phases B and C not modulated. During 0.2–1.2 s, the phase-A amplitude follows 11 kV × [1 + 0.5 sin(2π × 1 × (t − 0.2))]. It reaches about 1.5 p.u. near 0.45 s and about 0.5 p.u. near 0.95 s; Figure 7(c) shows DVR compensation.

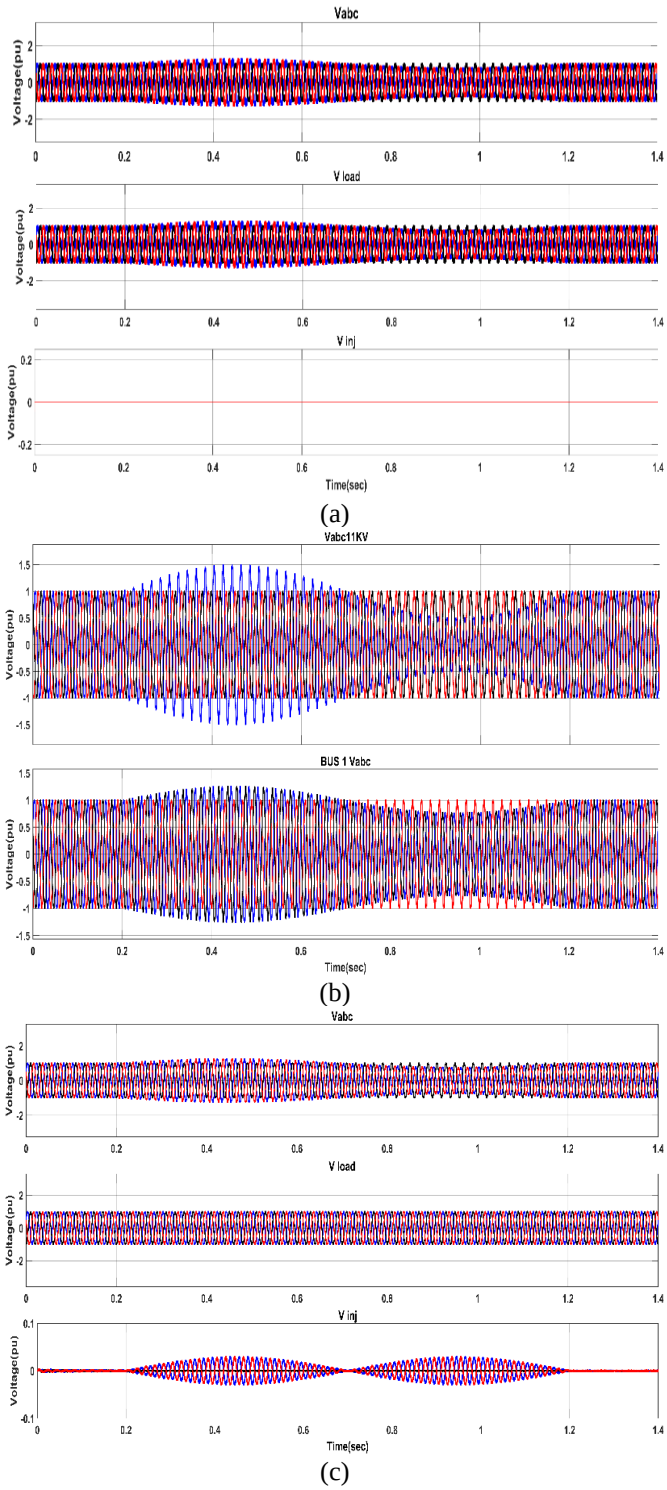


Figure 7. Voltages under programmed single-phase source-voltage modulation: (a) without the dynamic voltage restorer (DVR); (b) source-side phase voltages at the 11 kV bus and at BUS 1, each in per unit (p.u.) on its respective voltage base; (c) with DVR compensation

During the source-modulation rise (0.40-0.50 s) and drop (0.90-1.00 s), source-side VUFs were 14.0818% and 19.5932%, while the compensated BUS 2 values were 0.1473% and 0.1674%, respectively (Table 3). The corresponding mean phase RMS voltage errors after compensation were 0.1541% and 0.1522%. The residual fluctuation in Figure 7(c) is part of the expected closed-loop response: the PI loop has finite bandwidth, and the disturbance is a continuously varying 1 Hz amplitude modulation, so the load voltage follows it with a small residual error. The compensated mean RMS errors of 0.1541% and 0.1522% in the rise and drop windows bound this residual. The three-phase dynamic-load block is a balanced positive-sequence representation and does not produce this single-phase source disturbance.

For the separate switched-load test, the grounded-wye base load had phase active powers of 600/500/400 W (A/B/C) and inductive reactive powers of 200/170/130 var. A parallel phase-dependent load of 150/100/50 W and 50/30/20 var was connected at 0.35 s and disconnected at 0.85 s; capacitive power was zero. Nominal phase-power unbalance, defined as the maximum absolute departure from the three-phase mean divided by the mean, changed from 20%/22% to 25%/25% (active/reactive) and then returned to 20%/22%. Table 4 reports the corresponding measured load-voltage performance. During the connected interval, a low negative-sequence VUF coexisted with phase RMS deviations up to 12.4%; the measured 50 Hz zero-sequence magnitude was 14.1212% of the positive sequence, and the dq controller did not independently regulate the zero sequence. These observations do not establish a unique cause of the phase-voltage spread. No DVR-disabled benchmark was evaluated for this switched-load test, and complete phase-voltage restoration is not claimed.

8.5 Controller response and regulation limits

The investigated DVR uses the conventional discrete dq–PI controller described in Sections 5 and 6; this study evaluates its performance under the specified fault, source-modulation and switched-load conditions rather than proposing a new control method. Table 3 compares source-side and compensated load-side VUFs, and reports mean compensated RMS errors. A separate controller-to-controller reference comparison was not simulated, so comparative superiority is not claimed.

To quantify the dynamic response, we evaluated the exported inverter-side phase-to-ground voltage (V_{inj}), measured before the series injection transformer, using a trailing 1 ms RMS window, a 0.01 p.u. threshold, and a 2 ms persistence condition. After fault initiation at 0.05000 s, the first sustained above-threshold instants in the affected phases were 0.05008 s for SLG (phase A), 0.05006 s for LL (phases A and B), and 0.05004 s for LLG phase B (0.05008 s for phase A). After fault clearance at 0.25000 s, all affected inverter-side phases remained below this threshold from 0.25378 s (SLG), 0.25222 s (LL), and 0.26036 s (LLG). These post-processed threshold crossings characterise inverter-side voltage activity, not a separate fault-detection latency or direct measurements of physical line-side injection.

Load-voltage recovery was assessed separately using trailing one-cycle RMS magnitudes (20 ms at 50 Hz), with an acceptance band of 0.95-1.05 p.u. for all three load phases and a one-cycle persistence requirement. For SLG, LL, and LLG,

the computed load-phase RMS values remained within this band throughout 0.07–0.25 s. Because the moving RMS window averages the voltage across the disturbance onset, and no distinct out-of-band-to-in-band transition was resolved, a numerical load-voltage recovery or settling time cannot be established from this criterion; none is claimed.

Table 4. Switched-load phase-power unbalance and compensated load-voltage performance

Window (s)	P/Q Unbalance (%)	VUF after (%)	Mean RMS Error (%)	Phase RMS A/B/C (p.u.)
0.25–0.33	20/22	0.2067	6.4417	0.9032/0.9985/1.0949
0.40–0.50	25/25	0.4076	8.4020	0.8758/1.0037/1.1241
0.90–1.00	20/22	0.2255	6.5448	0.9079/1.0035/1.1008

Note: P and Q denote active and inductive reactive phase powers, respectively; unbalance is the maximum absolute departure from the phase mean divided by that mean. VUF = voltage-unbalance factor; RMS = root-mean-square; p.u. = per unit. Values are compensated load-side measurements, not a dynamic voltage restorer (DVR)-disabled comparison.

The measured load-side VUFs during SLG, LL, and LLG faults were 0.4426%, 0.5919%, and 0.3866%, respectively, with mean phase RMS voltage errors of 0.8983%, 0.9921%, and 1.2517% (Table 3). Under the programmed single-phase source-voltage modulation, the two evaluation windows gave load-side VUFs of 0.1473% and 0.1674%, with mean errors of 0.1541% and 0.1522%, respectively. These existing measurements and the inverter-side threshold observations above document regulation under the simulated operating conditions. The switched-load test had a larger mean RMS error of 8.4020% during load connection (Table 4). Consequently, the fault and source-modulation error bounds cannot be generalised to all unbalanced-load conditions. The results do not provide a small-signal stability proof, gain or phase margins, or a measured 2% settling time. Related zero-sequence DVR approaches are reported [19, 20].

9. CONCLUSIONS

This study evaluated the conventional discrete dq-PI-controlled DVR under three asymmetrical faults, programmed single-phase source-voltage modulation, and unbalanced load switching. The voltage unbalance factor decreased from 53.1844% to 0.4426%, from 97.3796% to 0.5919%, and from 93.3615% to 0.3866% in the fault cases. During the two programmed source-modulation windows, it decreased from 14.0818% to 0.1473% and from 19.5932% to 0.1674%; corresponding post-compensation mean RMS errors over all five intervals were 0.8983%, 0.9921%, 1.2517%, 0.1541%, and 0.1522%. These metrics document fundamental negative-sequence regulation but not comparative superiority, analytic stability margins or hardware validation. In the switched-load test, the connected-load mean RMS error was 8.4020%, and the phase-magnitude error reached about 12%, consistent with an unregulated zero-sequence component; the cause was not isolated. The transformer model is linear and does not saturate; the fault cases exceed its nominal winding settings, requiring further hardware-oriented verification. The synchronised PWM ratio exceeds the discrete update resolution and does not support a switching-harmonic claim.

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NOMENCLATURE

e_d, e_q	d- and q-axis load-voltage errors (p.u.)
$K_{p,d}$, $K_{p,q}$	proportional gains of the two PI controllers
$K_{i,d}$, $K_{i,q}$	integral gains of the two PI controllers
t	time (s)
u_a, u_b, u_c	three-phase inverter modulation commands
u_d, u_q	d- and q-axis PI output commands
u_α, u_β	stationary-frame commands
v_a, v_b, v_c	measured phase-to-ground load voltages (p.u.)
v_d, v_q	d- and q-axis measured load voltages (p.u.)
$v_{inj,abc}$	physical series-injected three-phase voltage (V)
$v_{load,abc}$	three-phase load voltage (V)
$v_{source,abc}$	three-phase source voltage (V)
v_α, v_β	stationary-frame measured voltage components (p.u.)
V_{LL}	nominal line-to-line rms voltage (V)
θ	PLL electrical angle (rad)