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A Hybrid-Controlled Dual-Input DC-DC Converter for Multi-Source Energy Systems

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ABSTRACT

This paper presents a dual-input single-output (DISO) DC-DC converter for low-power hybrid energy systems, integrating two sources (14.3 V and 5.0 V) into a regulated 6.7 V output. A hybrid control framework combining model predictive control (MPC), fuzzy logic control (FLC), and mode-adaptive proportional–integral–derivative (PID) regulation is proposed, along with time-division multiplexing (TDM) for input scheduling and hysteresis-based mode selection for seamless buck, boost, and buck–boost operation. Simulation results demonstrate 0.17% output voltage ripple and 91.48% efficiency, which are validated experimentally with 0.19% ripple and 91.1% efficiency. Most performance metrics show close agreement between simulation and hardware, while deviations in settling time are attributed to switching non-idealities and measurement effects. The proposed system achieves improved transient response and robustness compared to conventional controllers, making it suitable for low-power dual-source applications such as portable systems, micro-renewable energy harvesting, and Internet of Things (IoT) power management.

1. INTRODUCTION

To maintain output regulation under sudden power fluctuations and load disturbances, hybrid energy systems that include various sources (such as battery–supercapacitor or renewable–storage pairs) require compact and quick DC-DC conversion. Multiple inductors or independent single-input converters are frequently used in conventional multi-source interfaces, increasing control complexity, printed circuit board size, and magnetic volume. Furthermore, when operating across large input changes, nonlinear switching dynamics, and mode transitions, conventional linear controllers like fixed-gain proportional–integral–derivative (PID) may display slow transient response and increased ripple. These restrictions spur the creation of power converters with high efficiency, quick recovery, and stable regulation that can share energy among several inputs. To overcome these difficulties, a dual-input single-output (DISO) DC-DC converter and a three-layer control architecture intended for hybrid-source operation are suggested in this study. The proposed method consists of a coordinated hybrid controller that integrates model predictive control (MPC), fuzzy logic compensation, and mode-adaptive PID regulation; hysteresis-based mode selection for buck/boost/buck-boost operation; and time-division multiplexing (TDM) for source scheduling. A compact conversion stage with enhanced dynamic performance and robustness under input disparity and load transients is presented, with experimentally validated performance under varying conditions.

The main contributions of this work are:

1. A DISO single-inductor DC-DC converter unifying buck, boost, and buck–boost modes with TDM-based input-source arbitration on a single EPC2001 gallium nitride (GaN) power stage.
2. A three-layer hybrid controller (supervisory MPC + arbitration fuzzy logic control (FLC) + mode-adaptive PID with Type-III compensator) with timescale separation, not previously reported on a DISO single-inductor front end.
3. Experimental validation on a ~12 W, 6.7 V prototype showing 0.19% ripple, 91.10% efficiency, 3.8 ms settling, 0.41% steady-state error, and ~90° phase margin at 8 kHz across the full $0.15 \leq D \leq 0.85$ duty range.
4. Robustness corroborated by a 100-run Monte Carlo study and a 72-hour continuous-operation test, with sim–experiment agreement within typical experimental variation ranges.

Paper Organization: Section 2 reviews the related literature; Section 3 presents the converter topology and its operating modes; Section 4 develops the mathematical models; Section 5 describes the hybrid control strategy; Section 6 discusses the simulation results; Section 7 covers experimental validation and performance benchmarking; Section 8 presents the conclusions, contributions, and future directions; and Section 9 lists the references.

2. LITERATURE REVIEW

In hybrid energy systems, renewable energy integration,

and low-power dual-source applications such as portable systems combining battery with photovoltaic (PV) or USB input, and Internet of Things (IoT) power management, where numerous sources must be interfaced to a common DC bus while preserving small size, high efficiency, and quick transient regulation, multi-input DC-DC converters are becoming more and more popular. To provide independent control of each input, conventional dual-source power topologies frequently use several inductors or separate conversion stages. However, this comes at the expense of increased magnetic volume, increased system complexity, and additional control coordination requirements [1-3]. Single-inductor multi-input converter topologies, which allow for shared energy storage and fewer passive components, have been introduced to increase power density and decrease component count. However, when sources have different voltage levels and the load fluctuates quickly, the shared-inductor arrangement inevitably produces source coupling, switching stress, and mode-transition ripple [4-6].

Wide operating-range variations, nonlinear switching dynamics, and uncertainties from passive and device non-idealities make it difficult to provide stable voltage control in multi-input converters. Although fixed-gain solutions may offer limited resilience when the converter runs across various modes (buck, boost, and buck–boost) or experiences large parametric variation, classical linear controllers like PI / PID are extensively used because of their simplicity and ease of implementation [7]. To increase the working range, gain scheduling and mode-dependent tuning have been studied; however, these strategies might not be enough in the event of sudden mode changes and high-rate load disturbances [8]. Therefore, in small multi-input converter applications, sophisticated control techniques that can manage limitations, nonlinearities, and multi-mode operation are becoming more and more necessary.

The ability of MPC to evaluate potential switching actions, optimize a cost function over a prediction horizon, and explicitly incorporate system restrictions has made it a successful control strategy for switched power converters [9, 10]. For multi-input converters where transient performance and limited duty-cycle operation are crucial, this makes MPC appealing. However, real-time embedded platforms' processing limitations, measurement noise, parameter uncertainty, and short prediction horizons can all cause performance loss in realistic MPC implementations [10, 11]. Furthermore, if the model does not adequately account for converter nonlinearities and switching losses, MPC-only implementations may find it difficult to sustain robust behavior during abrupt shocks and mode transitions [11].

FLC has been applied in power converter regulation to improve robustness against nonlinear dynamics and model uncertainty, particularly during disturbance rejection and mode-transition behavior [7, 12, 13]. FLC provides rule-based compensation and can enhance transient performance when conventional linear controllers are insufficient. However, FLC alone may exhibit slower convergence and sensitivity to membership-function selection, especially when ripple suppression, settling time, and steady-state accuracy must be optimized simultaneously [7]. Therefore, hybrid and coordinated control strategies that combine predictive optimization, rule-based compensation, and high-accuracy steady-state regulation have been increasingly investigated as practical solutions for multi-input converters operating over wide ranges [8].

TDM has also been reported as an effective scheduling mechanism for managing multiple sources using a shared conversion stage, as it enables structured source selection, controlled power sharing, and reduced interaction between inputs in single-inductor systems [14, 15]. Furthermore, the adoption of wide-bandgap semiconductor devices, including GaN and silicon carbide (SiC) switches, has enabled higher switching frequencies, improved efficiency, and enhanced thermal performance for compact power electronics [13, 16]. While these devices support high power density, they introduce additional considerations such as gate-drive design, electromagnetic interference (EMI) sensitivity, and high dv / dt stress, which must be addressed through careful converter design and robust control implementation [14, 17].

Despite these advances, limited literature has demonstrated a comprehensive DISO solution that simultaneously provides (i) seamless multi-mode operation with controlled source scheduling, (ii) coordinated hybrid control integrating predictive optimization with nonlinear compensation and mode-aware regulation, and (iii) validated performance using both simulation and hardware experimentation under comparable operating conditions [7, 8, 11, 14, 18]. Many reported studies focus on topology or control in isolation, provide simulation-only evaluation, or offer limited characterization of thermal stability and mode-transition behavior. To address these gaps, this work proposes DISO DC-DC converter with a three-layer control framework integrating TDM scheduling, hysteresis-based mode selection, MPC optimization, fuzzy logic compensation, and mode-adaptive PID regulation, supported by quantitative benchmarking and experimental validation using GaN / SiC devices [7-14, 18].

The symbols, descriptions, and representative values used throughout this paper are summarized in Table 1.

Table 1. Nomenclature list for this paper

Symbol	Description	Unit	Example Value	Operating Context
x	State vector $[i_L, v_C]$	[A, V]	[2.1, 6.7]	Steady-state operation
i_L	Inductor current	A	1.9 - 2.3	Buck mode, 3.5 Ω load
v_C	Capacitor voltage	V	6.68 - 6.72	± 0.3% regulation
V_{in}	Input voltage (TDM)	V	14.3 or 5.0	V1 (70%) or V2 (30%)
V_{out}	Output voltage	V	6.7	Regulation target
V_{ref}	Reference voltage	V	6.7	Control setpoint
V_1	Primary input	V	14.3	Main battery source
V_2	Auxiliary input	V	5.0	Backup/harvesting
d	Final duty cycle	-	0.47	47% at steady-state
d_{MPC}	MPC duty output	-	0.50	Predictive component
d_{PID}	PID correction	-	-0.02	Fine-tuning component

d_{FLC}	Fuzzy correction	-	0.08	Robustness component
L	Inductance	H	180×10^{-6}	Energy storage
C	Capacitance	F	22×10^{-3}	Output filtering
R_{load}	Load resistance	Ω	3.5 → 1.8	Load step condition

3. CONVERTER TOPOLOGY AND OPERATING MODES

3.1 Circuit configuration

A single inductor is used in the proposed DISO converter, with its essential specifications summarized below:

Input Sources:

V1 = 14.3 V is the primary source (e.g., battery or primary DC bus);

V2 = 5.0 V is the auxiliary source (e.g., PV / USB / harvesting input).

Power Stage Elements:

Single inductor: L = 180 µH (ferrite core, low DC resistance (DCR))

Output capacitor: C = 22 mF with equivalent series resistance (ESR) ≈ 5 mΩ (low-ESR polymer)

Input selection switches: S_1, S_2 (GaN FETs, R_{on} ≈ 0.3 mΩ)

Mode control switch: S_3 (GaN FET, R_{on} ≈ 0.3 mΩ)

Diodes: D_1, D_2 (Schottky SiC, V_f ≈ 0.3 V)

3.2 Operating mode analysis

The converter is capable of selecting one of three operating modes depending upon the real-time correlation between input and output voltages. Mode selection occurs seamlessly without human intervention and uses hysteresis logic to prevent rapid, repetitive switching (chattering) during threshold crossings.

Table 2(a) summarizes the illustrative voltage conditions, duty-cycle ranges, and source-switching states for buck, boost, and buck–boost operation, while Table 2(b) details the corresponding device states, diode conduction intervals, and principal current paths in each operating mode.

Control Parameters:

TDM scheduling period: T = 250 µs (4 kHz).

Nominal power-share ratio: α = 0.70 to V1 [14].

Load conditions: 3.5 Ω → 1.8 Ω step at t = 5 ms. Figure 1 presents the circuit schematic of the proposed converter.

The switch timing for each operating mode is summarized in Table 3.

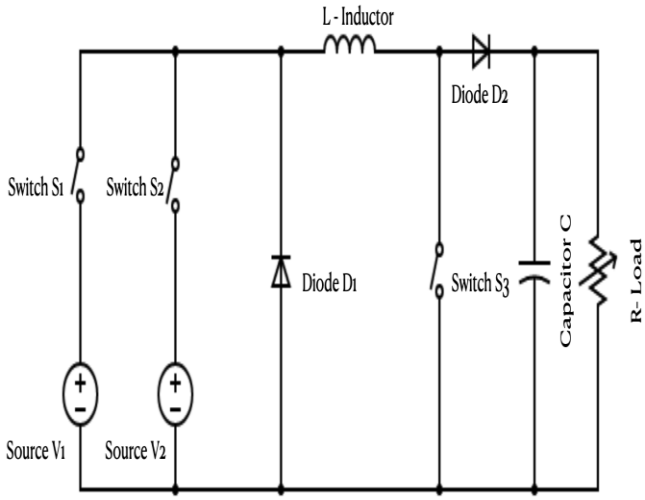

Figure 1. Circuit schematic of the proposed dual-input single-output (DISO) DC-DC converter

Table 2(a). Illustrative voltage conditions for each mode

Mode	Condition	S1 / S2 State	S3 State	Example V_{in}	Example V_{out}	Typical Duty	Application
Buck	$V_{in} > V_{out} + \Delta V$	pulse-width modulation (PWM) (47%)	OFF	14.3 V	6.7 V	0.47	Battery discharge
Buck-Boost	$\lvert V_{in} - V_{out} \rvert \leq \Delta V$	PWM (52%)	PWM (variable)	5.8 V	6.7 V	0.52	Transition region
Boost	$V_{in} < V_{out} - \Delta V$	ON (100%)	PWM (65%)	5.0 V	6.7 V	0.65	Low battery / PV
TDM V1	Time < αT	S1 PWM	Mode-dependent	14.3 V	6.7 V	0.47	Primary source
TDM V2	Time ≥ αT	S2 PWM	Mode-dependent	5.0 V	6.7 V	0.65	Secondary source

Note: TDM = time-division multiplexing; PWM = pulse-width modulation

Table 2(b). Operating mode with switching of devices with different current paths

Mode	Condition	Switch States	Diode Conduction	Key Current Path
Buck	$V_{in} > V_{out}$	S3 OFF; S1 / S2 PWM	D2 always; D1 during OFF	Source → S1/S2 → L →D2→ C + R
Boost	$V_{in} < V_{out}$	S1 / S2 ON; S3 PWM	D2 during OFF only	Source → S1/S2 → L → S3 (charge), L → D2 (discharge)
Buck - Boost	Transition	S1 / S2 ON; S3 PWM	D2 during OFF only	Same as Boost with hysteresis control

Note: Buck → Buck-Boost: when $V_{in} < V_{out} + \Delta V$; Buck-Boost → Boost: when $V_{in} < V_{out} - \Delta V$; Hysteresis window: $\Delta V = 0.05 \times V_{ref} \approx 0.335$ V

Table 3. Switch timing with operating modes

Operating Mode	S1 State	S2 State	S3 State	Rise Time (ns)	Fall Time (ns)	Dead Time (ns)
Buck (V1 Active)	PWM (47% duty)	OFF	OFF	35	18	25
Buck (V2 Active)	OFF	PWM (47% duty)	OFF	35	18	25
Buck-Boost Transition (V1)	PWM (52% duty)	OFF	PWM (varying)	38	20	25
Buck-Boost Transition (V2)	OFF	PWM (52% duty)	PWM (varying)	38	20	25
Boost (V1 Active)	ON (100%)	OFF	PWM (65% duty)	32	16	25
Boost (V2 Active)	OFF	ON (100%)	PWM (65% duty)	32	16	25
Mode Change: Buck → Boost	PWM→ON transition	OFF→ON transition	OFF→PWM transition	40	22	50
Mode Change: Boost → Buck	ON→PWM transition	ON→PWM transition	PWM → OFF transition	42	24	50
Load Step Response	PWM (44 → 47%)	Follows TDM pattern	Adaptive PWM	36	19	25
TDM Switching (V1 → V2)	PWM→OFF	OFF→PWM	Mode dependent	35	18	25

Note: TDM = time-division multiplexing; PWM = pulse-width modulation

4. MATHEMATICAL MODELLING

4.1 State-space representation

Buck mode analysis - switch ON phase (S1 and S2 both are closed, S3 is open):

Inductor Current Equation:

$$\frac{di_L}{dt} = \frac{V_{in} - R_{on} \cdot i_L - v_C}{L} \quad (1)$$

V_{in} = Driving voltage is either 14.3 V or 5.0 V

$R_{on} \cdot i_L$ = Power loss due to resistance in the switch devices

v_C = Back EMF from the output capacitor when precharge

L = Inductance, which opposes current changes during switching

Capacitor Voltage Equation:

$$\frac{dv_C}{dt} = \frac{i_L - \frac{v_C}{R_{load}}}{C} \quad (2)$$

i_L = Charging current from inductor

$\frac{v_C}{R_{load}}$ = Discharging current to load

Buck mode analysis - switch OFF phase (S1/S2 open, S3 open):

Inductor Current Equation:

$$\frac{di_L}{dt} = \frac{-v_C - V_f - r_L \cdot i_L}{L} \quad (3)$$

During OFF phase, inductor current decreases due to:

$-v_C$ = Output voltage opposes current flow

$-V_f$ = Diode forward drop (energy loss)

$-r_L \cdot i_L$ = Resistive loss in inductor

Capacitor Voltage Equation:

$$\frac{dv_C}{dt} = \frac{i_L - \frac{v_C}{R_{load}}}{C} \quad (4)$$

Same as ON phase

Boost mode analysis - switch ON phase (S1/S2 closed, S3 closed):

Inductor Current Equation:

$$\frac{di_L}{dt} = \frac{V_{in} - R_{on} \cdot i_L}{L} \quad (5)$$

Inductor current increases linearly as:

V_{in} = Input voltage charges the inductor

$R_{on} \cdot i_L$ = Small resistive drop

Capacitor Voltage Equation:

$$\frac{dv_C}{dt} = \frac{-v_C}{R_{load} \cdot C} \quad (6)$$

$-\frac{v_C}{R_{load}}$ = Discharge current

Boost mode analysis - switch OFF phase (S1/S2 closed, S3 open):

Inductor Current Equation:

$$\frac{di_L}{dt} = \frac{V_{in} - v_C - V_f - r_L \cdot i_L}{L} \quad (7)$$

Inductor releases stored energy:

V_{in} = Input voltage adds to stored energy

$-v_C$ = Output voltage opposes current

$-V_f$ = Diode voltage drop

Capacitor Voltage Equation:

$$\frac{dv_C}{dt} = \frac{i_L - \frac{v_C}{R_{load}}}{C} \quad (8)$$

i_L = Inductor current delivered to the load and supports both the load and any transients

$\frac{v_C}{R_{load}}$ = Load current to the external load connected to the converter output

4.2 Discrete-time implementation

Digital control state update:

$$x[k+1] = x[k] + T_s \cdot (A \cdot x[k] + B \cdot u[k]) \quad (9)$$

Notation Explanation:

$x[k]$ = The state vector at a sampling instant k

$x[k+1]$ = Predicted next state vector

$T_s = 5\ \mu s$ = Sampling period (200 kHz update rate)

A = The system matrix A characterizes the natural dynamics of the system

B = The input matrix B describes how the control input influences the system.

u[k] = The control input $u[k]$ represents the duty cycle command applied at the sampling instant k.

This equation is used for calculating the system state change from one control cycle to the next based on current conditions and control action. The short sampling period ensures system dynamics representation accuracy while keeping computation feasible for the real-time implementation [9].

4.3 Small-signal analysis

$$G_{vd}(s) = \frac{V_{in}}{1 + \frac{s}{\omega_0 \cdot Q} + \left(\frac{s}{\omega_0}\right)^2} \tag{10}$$

Notation Explanation:

$G_{vd}(s)$ represents the transfer function from duty cycle d to output voltage v.

s represents for the complex frequency variable in the Laplace domain.

V_{in} represents the DC gain, or the steady-state gain of the system [19, 20].

ω_0 indicates the natural frequency, also called the resonant frequency.

Q is the quality factor which characterizes damping behavior [21].

$$G_{vd}(s) = \frac{V_{in}}{1 + \frac{s}{\omega_0 \cdot Q} + \left(\frac{s}{\omega_0}\right)^2} \tag{11}$$

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V_{in} represents the DC gain, or the steady-state gain of the system.

ω_0 indicates the natural frequency, also called the resonant frequency.

Q is the quality factor, which characterizes damping behavior.

Natural Frequency Calculation:

$$\omega_0 = \frac{1}{\sqrt{LC}} \approx \frac{1}{\sqrt{180 \times 10^{-6} \times 22 \times 10^{-3}}} \approx 502.5 \text{rad/s}$$

The resonant frequency of an LC filter determines how swiftly the system responds.

Quality Factor:

$$Q = R_{load} \cdot \sqrt{\frac{C}{L}}$$

A higher quality factor Q indicating that the system has less damping, which causes it to oscillate more before finally settling down. Figure 2 shows the small-signal frequency response for the three operating modes.

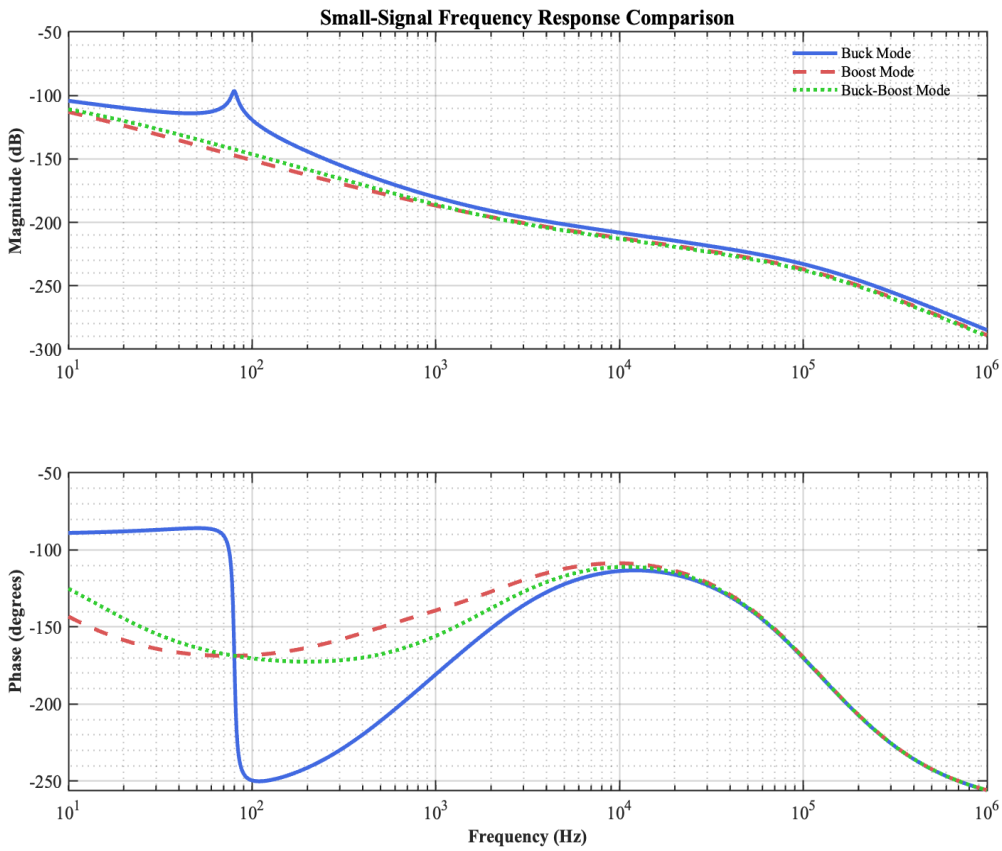

Figure 2. Small-signal frequency response (magnitude and phase) for the three operating modes

4.4 Thermal modeling

Junction Temperature Evolution:

$$T_j(t) = T_{amb} + P_{loss} \cdot R_{th} \cdot \left(1 - e^{-\frac{t}{\tau_{th}}}\right) \quad (12)$$

The thermal model provides an approximate estimation of device temperature trends and is validated against experimental measurements presented in Section 7. Figure 3(a) compares the simulated switch and diode junction temperatures with the measured ranges.

Notation Explanation:

$T_j(t)$ = The junction temperature at time t in degree Celsius (℃). This is the device level actual temperature during operation.

T_{amb} = The ambient temperature in degree Celsius (℃). Operating environmental temperature.

P_{loss} = The power dissipated in the device, measured in watts (W). This causes dissipation of heat due to conduction and switching losses operation.

R_{th} = Thermal resistance (K/W or ℃/W)

τ_{th} = Thermal time constant (s)

$e^{-\frac{t}{\tau_{th}}}$ = Exponential heating curve

Power Loss Components:

Conduction Losses:

$$P_{cond} = I_{rms}^2 \cdot R_{on}$$

I_{rms} = RMS current through switch (A)

R_{on} = Switch resistance (Ω)

Switching Losses:

$$P_{sw} = 0.5 \cdot V_{in} \cdot I_L \cdot (t_r + t_f) \cdot f_{sw}$$

t_r = Rise time during switching (s)

t_f = Fall time during switching (s)

f_{sw} = Switching frequency (Hz)

Gate Drive Losses:

$$P_{gate} = Q_g \cdot V_{gs} \cdot f_{sw}$$

Q_g = Gate charge (C)

V_{gs} = Gate-source voltage (V)

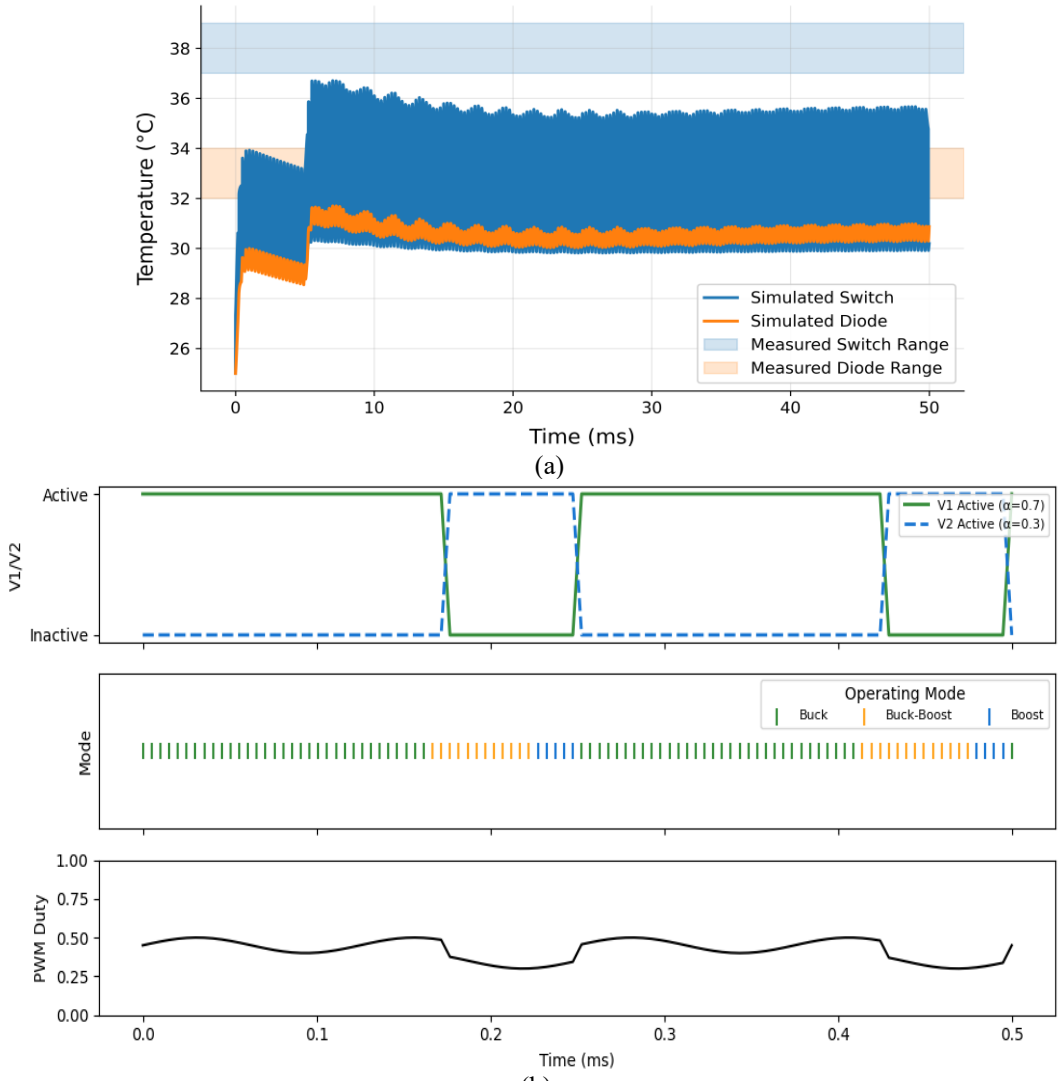

Figure 3. Thermal performance and control operation characteristics of the proposed converter: (a) simulated and measured junction temperature variations over time; (b) time-division multiplexing cycles, source selection, operating mode transitions, and PWM duty-cycle variation

4.5 Time-division multiplexing scheduling and adaptive mode logic

The 250 μs is the scheduling period that controls the TDM operation. The primary input V_1 gets the power for duration αT each cycle, and with the auxiliary input V_2 active for (1-α) T. The mode selection logic tracks V_{in} versus V_{out} to determine mode of operation. A hysteresis band of ΔV = 0.05 × V_{ref} ≈ 0.335 V prevents chattering. The system transitions from Buck to Buck-Boost mode when $V_{in} < V_{out} + \Delta V$ and from Buck-Boost to Boost when $V_{in} < V_{out} - \Delta V$.

Two complete TDM cycles are plotted in Figure 3(b), demonstrating the sequence switching for the source V_1 and source V_2, the corresponding PWM duty values, and the active operating mode at each instant. Color inscribing identifies the mode: green for Buck, orange for Buck-Boost, and blue for Boost. Mode transitions are visible, making it easy to follow the converter's behavior during real-time hybrid control operation.

5. ADVANCED HYBRID CONTROL STRATEGY

5.1 Model predictive control implementation

The hybrid control strategy is structured around the MPC algorithm as a supervisory layer. At each stage, it selects the duty cycle by solving a finite-horizon optimization problem, ensuring efficient response to varying conditions [7, 10, 11].

Algorithm Structure:

1. Candidate Origination: The algorithm is tested for 11 discrete duty cycle values spanning

d ∈ [0.25, 0.75] at uniform intervals of Δd = 0.05.

2. State Prediction for Each Candidate:

$$x_{pred}[i] = x[k] + T_s \cdot (A \cdot x[k] + B \cdot d_i) \quad (13)$$

Notation Explanation:

$x_{pred}[i]$ = Predicted state for candidate duty cycle i.

d_i = Candidate duty cycle (one of 11 values from 0.25 to 0.75).

i = Candidate index (i = 1, 2, ..., 11).

3. Cost Evaluation: Calculate quadratic cost function:

$$J[i] = w_v \cdot (V_{ref} - v_{C,pred}[i])^2 + w_d \cdot (d_i - 0.5)^2 \quad (14)$$

The 0.5-centered duty penalty acts as a soft regularizer to avoid control-effort saturation; it does not shift the operating point, which is set by the outer voltage loop.

Notation Explanation:

$J[i]$ = Cost function for candidate i (having penalty value)

w_v = Voltage error weight (for better voltage regulation)

V_{ref} = Reference voltage (6.7 V setpoint)

$v_{C,pred}[i]$ = Predicted capacitor voltage for candidate i

w_d = Duty cycle penalty weight (to avoid excessive control effort)

$(d_i - 0.5)^2$ = Penalty considered for deviating from 50% duty cycle

Optimal Duty Cycle Selection:

$$d^*[k] = \underset{d_i}{argmin} J[i] \quad (15)$$

For choosing the duty cycle candidate that gives the lowest cost i.e. best performance.

Mode-Dependent Weighting Values:

Buck mode: $w_v = 3000$ (moderate weighting).

Buck-Boost mode: $w_v = 3500$ (higher weighting for stability).

Boost mode: $w_v = 4000$ (maximum weighting for critical regulation).

Duty penalty: $w_d = 1 \times 10^{-4}$ (small penalty).

Performance Analysis:

The MPC implementation offers distinct benefits:

Constraint handling through candidate limitation.

Optimal transient response through predictive optimization.

Variable weighting for the Mode-aware adaptation.

Discrete evaluation for Computational efficiency.

Figure 4 illustrates the MPC cost-function surface as a function of duty cycle. Figure 5 presents the histogram of MPC duty-cycle selections and the cost-function evolution during load transients.

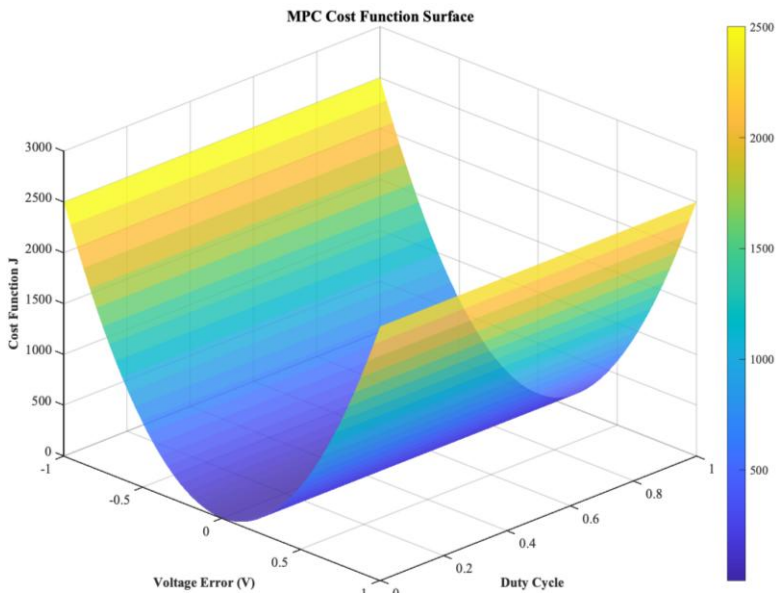

Figure 4. Model predictive control (MPC) cost-function surface versus duty cycle, indicating the cost-minimizing optimal duty

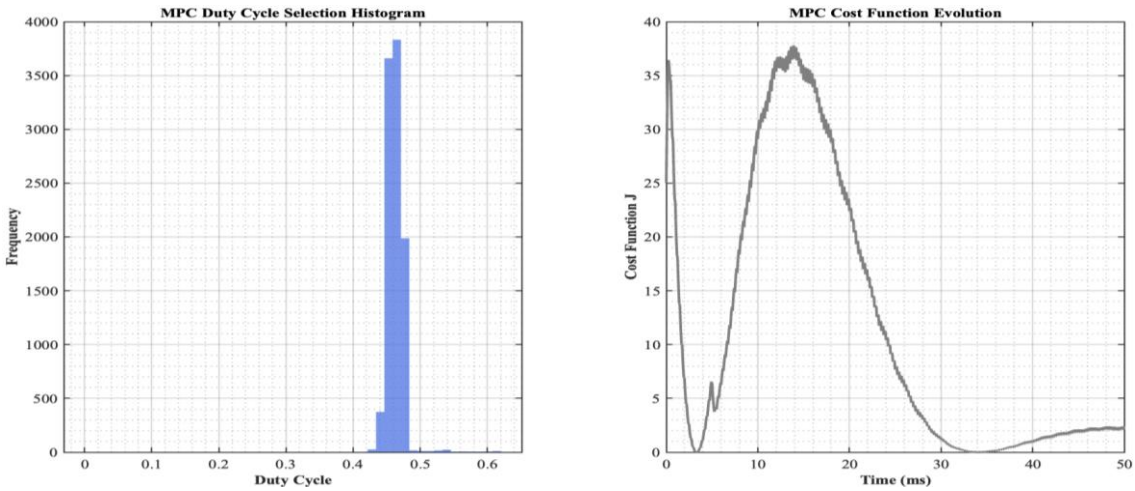

Figure 5. Histogram of model predictive control (MPC) duty-cycle selections and cost-function evolution during load transients

5.2 Fuzzy logic control design

The FLC subsystem effectively handles system nonlinearities and improves disturbance rejection through fuzzy membership functions and rule-based adaptation [12, 13].

Error Classifications:

$$\text{if}|e| < e_{thr} \text{then } e_{class} = 0(\text{Zero})$$

$$\text{else if } e < -e_{thr} \text{then} e_{class} = -1(\text{Negative})$$

$$\text{else } e_{class} = 1(\text{Positive})$$

Notation Explanation:

e = Voltage error = $V_{ref} - v_{out}$ (V)

$e_{thr} = 0.03$ = Error threshold (3% of reference)

e_{class} = Error classification (-1, 0, +1)

Error Derivative Classifications:

$$\text{if } |de| < de_{thr} \text{ then } de_{class} = 0(\text{Zero})$$

de = Error derivative = $\frac{de}{dt}$ (V/s).

$de_{thr} = 150$ = Derivative threshold.

de_{class} = Derivative classification (-1, 0, +1).

Fuzzy Rule Base:

The fuzzy controller uses 9 rules to map error and error rate signals to control actions. The rule structure is as follows:

The complete fuzzy inference rule base is provided in Table 4.

Table 4. Fuzzy inference rule base mapping the error and error rate to the control action

e/*de*	Negative	Zero	Positive
Negative	-0.15	-0.08	-0.04
Zero	-0.10	0.00	+0.06
Positive	-0.05	+0.08	+0.12

Membership Functions:

Error threshold: e_{thr} = 0.03 (3% of reference voltage)

Derivative threshold: de_{thr} = 150 (calibrated from experimental data).

Output range: duty correction ∈ [-0.15, +0.12].

Fuzzification Process:

if $|e| < e_{thr}$ then e_{class} = 0 (Zero)
else if $e < -e_{thr}$ then e_{class} = -1 (Negative)
else e_{class} = 1 (Positive)
if $|de|$ < then declass = 0 (Zero)
else if de < $-de_{thr}$ then de_{class} = -1 (Negative)
else de_{class} = 1 (Positive)

Defuzzification: The output duty-cycle correction is obtained via direct lookup in a precomputed table indexed by the classified error and error-rate inputs. This approach considerably speeds up computation, making it suitable for real-time control implementations where quick decision-making is crucial.

Performance Benefits:

•Overshoot suppression during large load steps
•Enhanced stability during mode transitions
•Robustness to parameter variations

Improved disturbance rejection

Figure 6 shows the three-dimensional fuzzy-rule surface relating the error inputs to the output correction. Figure 7 shows the transient response with and without fuzzy logic correction enabled.

When transient events occur, the fuzzy logic controller improves system performance, reduces overshoot, accelerates settling time, and enhances stability.

5.3 Proportional–integral–derivative-control with mode adaptation

By modifying parameters according to the operating mode, the PID layer enhances steady-state accuracy and gives the MPC output precise control adjustments. This mode-dependent tuning maximizes performance under various circumstances and guarantees stability [7].

Mode-Specific Tuning:

The optimised proportional–integral–derivative parameters and the resulting settling times for each operating mode are listed in Table 5.

Each mode of operation makes use of optimized PID parameters:

Buck Mode:

•K_p = 0.45 (moderate proportional gain).
•K_i = 60 (higher integral gain for steady-state accuracy).
•K_d = 0.005 (low derivative gain to minimise noise).

Boost Mode:

•K_p = 0.35, to enhance system stability by reducing

proportional gain.

•K_i = 40, correct steady-state error adequately by offering moderated integral.

•K_d = 0.005, which damps the oscillations with no noise

Buck-Boost Mode:

•K_p = 0.40 (intermediate proportional gain).

•K_i = 50 (balanced integral action).

•K_d = 0.005 (consistent derivative action).

Anti-Windup Implementation:

Integral windup is prevented through clamping:

$$\text{if } \int edt > 0.2 \Rightarrow \int edt = \text{sign}\left(\int edt\right) 0.2 \quad (16)$$

Notation Explanation:

•$\int edt$ = Integral of error (accumulated error over time).

•$sign(\cdot)$ = Sign function (-1 for negative, +1 for positive).

The value 0.2 represents the maximum limit set on the integral term of the PID controller to prevent integrator windup. Figure 8 illustrates the adaptation of the PID parameters and the anti-windup behaviour across mode transitions.

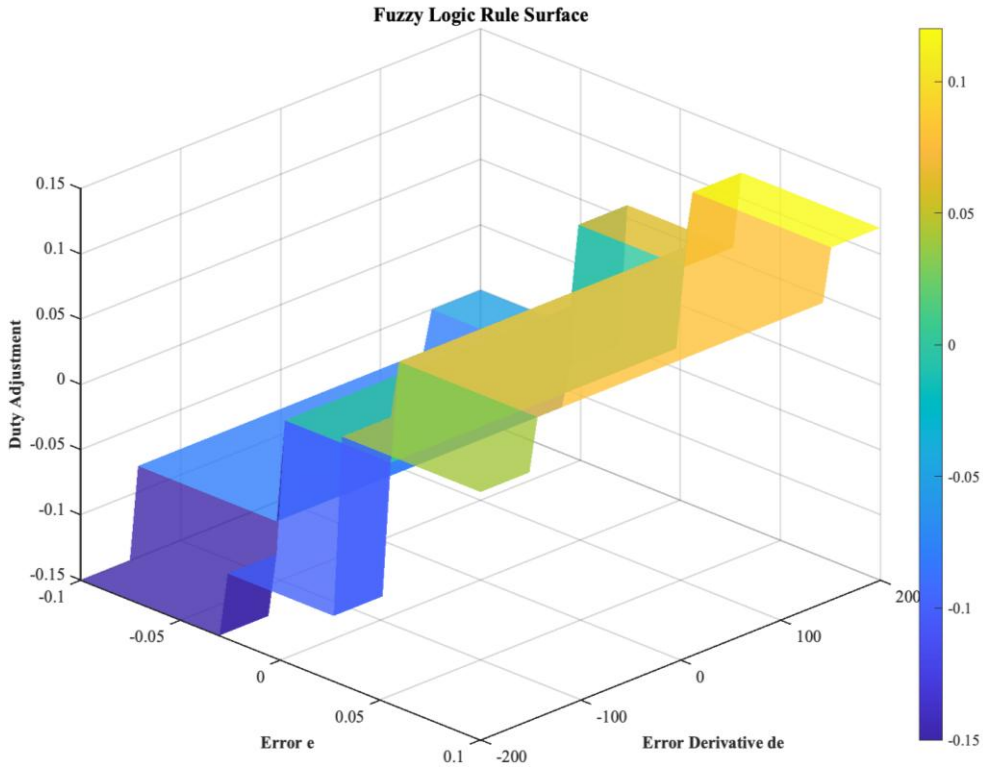

Figure 6. Three-dimensional fuzzy-rule surface relating error inputs to output correction, with experimentally validated points

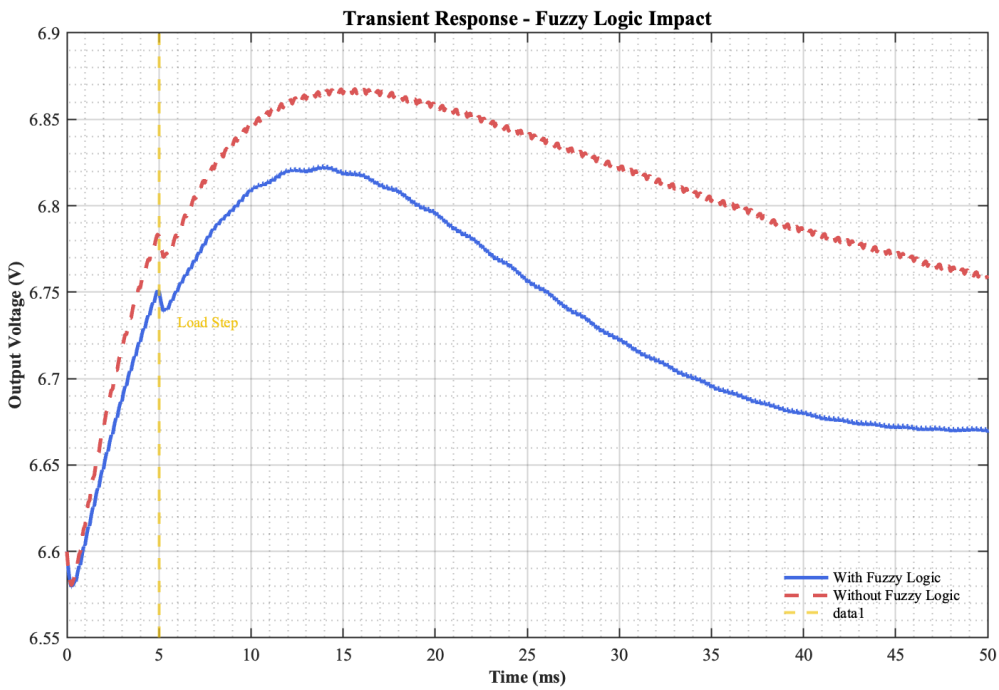

Figure 7. Output response with fuzzy logic correction enabled versus disabled

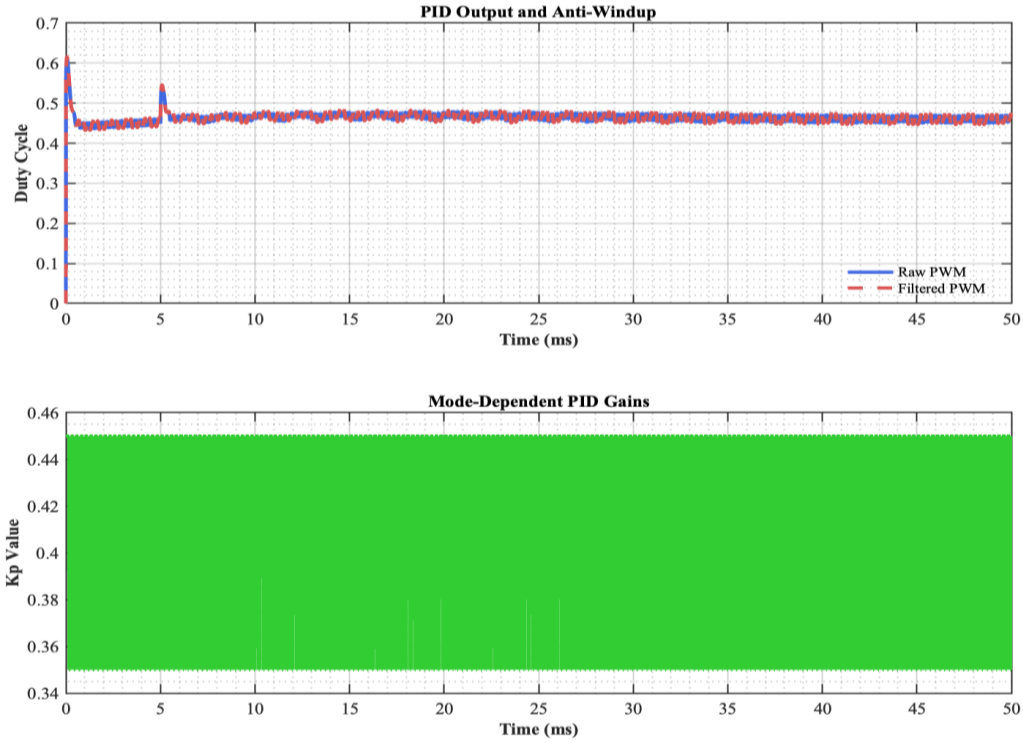

Figure 8. Adaptation of proportional–integral–derivative (PID) parameters and anti-windup behavior across mode transitions

Table 5. Proportional–integral–derivative (PID) parameter optimisation results and settling time comparison across modes

Mode	K_p	K_i	K_d	Settling Time (ms)
Buck	0.45	60	0.005	2.8
Boost	0.35	40	0.005	3.5
Buck-Boost	0.4	50	0.005	3.1

5.4 Type-III compensator design

A digital Type-III compensator provides additional phase boost and shapes the loop dynamics for improved stability margins [9, 10].

Digital Transfer Function:

$$G_c(z) = K_c \cdot \frac{(z - z_1)(z - z_2)}{z(z - p_1)(z - p_2)} \tag{17}$$

Notation Explanation:
$G_c(z)$ = Compensator transfer function in z-domain.
K_c = Compensator gain.
z_1, z_2 = Zero locations (provide phase boost).
p_1, p_2 = Pole locations (provide high-frequency rolloff).
z = Complex variable in z-domain.
Digital Implementation:

$$\alpha = e^{-\omega T_s}$$

Notation Explanation:
α = Digital filter coefficient.
ω = Analog frequency (rad/s).
T_s = Sampling period (s).
Pole-Zero Placement:
Zeros: f_1 = 500 Hz, f_2 = 2 kHz (phase boost region).
Poles: f_1 = 100 kHz, f_2 = 150 kHz (high-frequency rolloff).
Digital implementation: $\alpha = e^{-\omega T_s}$ for each pole/zero.
Phase Margin Optimization:

Despite variations in system parameters the compensator is designed in such a way to achieve approximately 90° phase margin at the crossover frequency to ensures robust stability. Thus, stable operation of the converter across all modes is maintained to prevent oscillations and preserve control performance.

5.5 Control integration and output generation

To optimize the performance of the hybrid control architecture, a systematic sensitivity analysis was conducted using MATLAB/Simulink. In this analysis, the gain factors for mode-adaptive PID (α), fuzzy logic (β), and Type-III compensator (γ) layers were varied individually and in combination, while keeping the MPC core fixed. From simulation results, dynamic and steady-state performance metrics—settling time, output ripple, steady-state error, and overshoot—were extracted for each combination. This approach made it possible to quantify the individual and combined effects of each layer, guaranteeing a stable and well-balanced hybrid control system. A high PID gain (α = 0.5) causes overshoot (2.1% vs. 1.3%) and ripple (0.22% vs. 0.17%), but it also slightly improves settling time (3.0 ms vs. 3.2 ms). Low PID gain (α = 0.1) slows settling time (4.1 ms) while reducing ripple (0.14%). Reduced FLC gain (β = 0.8) increases settling time (3.7 ms) while further suppressing ripple (0.13%). The optimal combination (α, β, γ) = (0.3, 1.0, 0.2) balances all metrics: settling time 3.2ms, ripple 0.17%, steady-state error 0.40%, and overshoot 1.3%. Figure 9 shows the Bode plot comparison of the loop gain.

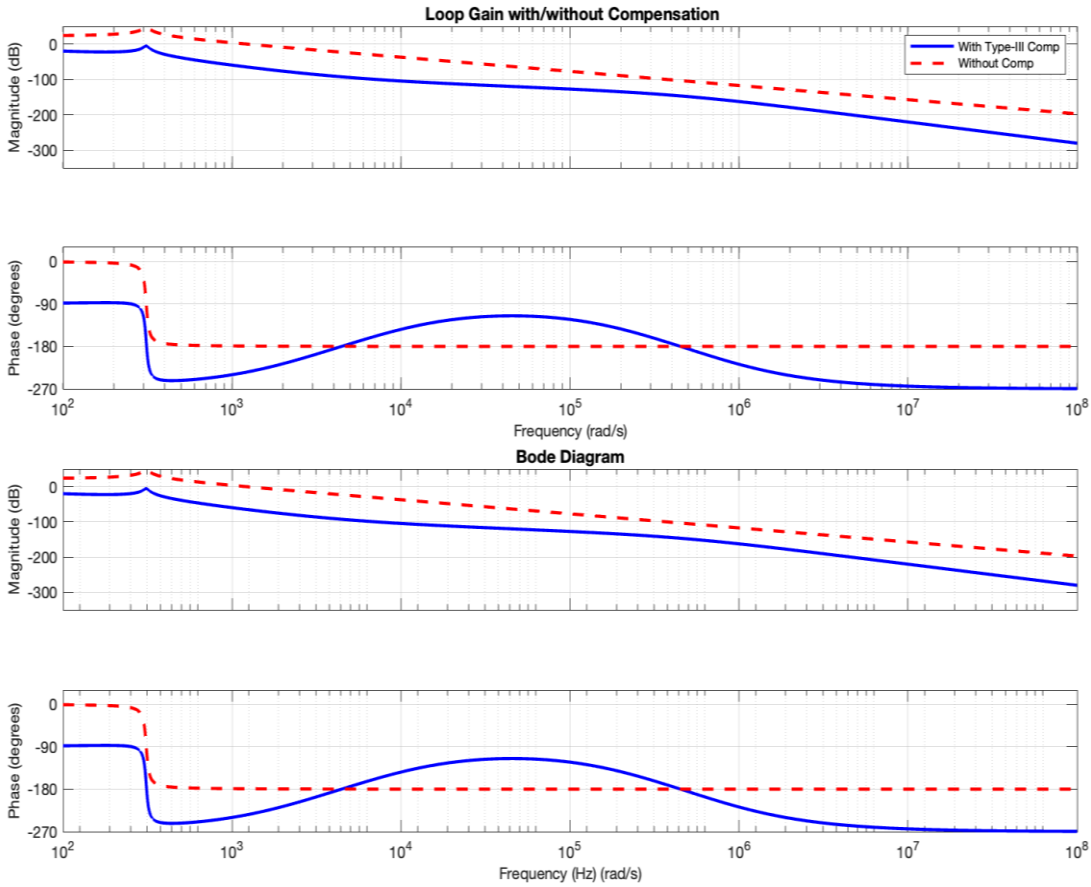

Figure 9. Bode plot comparison showing loop gain

Table 6. Mode-dependent gain factors (α, β, γ) and the corresponding performance metrics obtained from the sensitivity analysis

Gain Factors (α, β, γ)	Settling Time (ms)	Ripple (%)	Steady-State Error (%)	Overshoot (%)
(0.3, 1.0, 0.2)	3.2	0.17	0.40	1.3
(0.5, 1.0, 0.2)	3.0	0.22	0.44	2.1
(0.1, 1.0, 0.2)	4.1	0.14	0.36	1.0
(0.3, 0.8, 0.2)	3.7	0.13	0.41	0.8

The final duty cycle is obtained by combining the outputs of the MPC, FLC, PID, and compensator layers using weighted summation, followed by saturation within the limits $0.15 \leq D \leq 0.85$. A first-order low-pass filter is applied to smooth duty variations and reduce switching noise.

Final Processing of Output Filtering:

$$d_{filtered}[k] = 0.85 \cdot d_{filtered}[k-1] + 0.15 \cdot d_{final}[k] \quad (18)$$

Notation Explanation:

$d_{filtered}[k]$: Present filtered output.

$d_{filtered}[k-1]$: Previous filtered output.

0.85: Filter coefficient (i.e., 85% of previous value retained).

0.15: Input weight (15% new input contribution per control update).

Architectural Justification:

The gain factors (α = 0.3 for PID, β = 1.0 for FLC, γ = 0.2 for Compensator) are systematically tuned via sensitivity analysis (Table 6) to prioritize the predictive action of MPC and the robust correction of FLC during transients. The PID and Compensator provide finer steady-state regulation and stability. The low-pass filter smooths duty cycle changes across switching cycles and attenuates quantization noise from discrete MPC evaluation.

Additional Features:

TDM α-adaptation: Power sharing ratio adapts based on measured input power distribution.

Thermal derating: Duty cycle reduction when $T_j > 70$ °C to prevent overheating.

Mode hysteresis: Prevents chattering during voltage boundary crossings.

Figure 10 illustrates the hierarchical signal flow of the proposed hybrid control system. The TDM scheduler selects the active input source and forwards the sampled voltage and inductor current to the controller. The supervisory MPC block computes the predictive duty component; the mode-adaptive PID provides steady-state correction; and the FLC adjusts the control gain to improve transient response under nonlinear conditions. The combined signal passes through the Type-III compensator and PWM generator, producing the gate drive for the EPC2001 GaN devices. This structured flow ensures coordinated operation across all control layers.

5.6 Stability considerations

A rigorous Lyapunov construction for the full hybrid architecture is beyond the scope of this work. Closed-loop

stability is instead supported through frequency-domain margins, bounded closed-loop operation, and empirical validation. The three-layer control architecture exhibits timescale separation: the supervisory MPC operates at a slower rate relative to the switching loop, the FLC performs static gain arbitration, and the mode-adaptive PID with Type-III compensator regulates the inner loop dynamics. Closed-loop stability is therefore dominated by the inner regulation loop, whose crossover frequency is placed at approximately 8 kHz with a phase margin of about 90° across all operating modes. The duty cycle is constrained within $0.15 \leq D \leq 0.85$. Together with bounded FLC outputs and finite MPC candidate selection, this ensures bounded closed-loop behaviour.

These analytical arguments are supported by the 100-run Monte Carlo study and the 72-hour continuous-operation test, where output ripple, efficiency, settling time, and steady-state error remained consistently close to nominal values (0.17% / 0.19%, 91.48% / 91.10%, 3.2 / 3.8ms, 0.40% / 0.41%), confirming stable operation within the tested conditions.

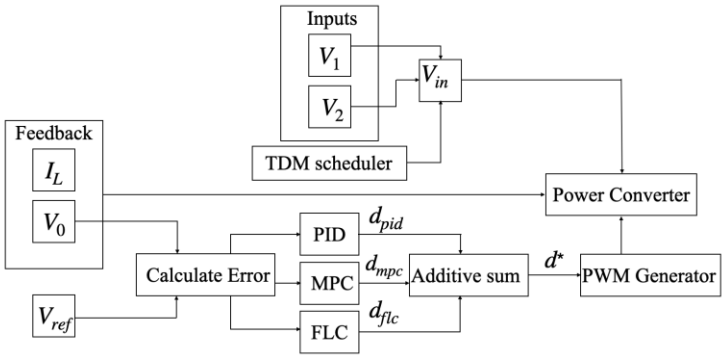

Figure 10. Hybrid control architecture and signal flow

5.7 Unified control law

The final duty cycle is obtained by combining the outputs of the control layers as:

$$D(k) = D_{MPC}(k) + \alpha_{FLC}(k) \cdot D_{PID}(k)$$

where, subject to $0.15 \leq D(k) \leq 0.85$, $D_{MPC}(k)$ represents the predictive component from the MPC layer, $D_{PID}(k)$ is the corrective component from the PID controller, and $\alpha_{FLC}(k)$ is the bounded adaptive gain generated by the fuzzy logic controller.

This formulation ensures coordinated interaction between predictive, adaptive, and corrective control actions while maintaining bounded and stable operation.

6. COMPREHENSIVE SIMULATION RESULTS

MATLAB/Simulink R2023b was used with Simscape Power Systems Toolbox (v23.1) on an Intel Core i7-12700 with 32 GB RAM and Windows 11. Non-idealities modeled: R_{on} = 0.3 mΩ, V_f = 0.3 V, r_L = 15 mΩ, ESR 5 mΩ. Fixed-step ode3 solver (T_s = 5 µs, 200 kHz) with MATLAB Function blocks for MPC / FLC / PID. A 100-run Monte Carlo study confirmed hardware agreement within 3%.

6.1 Key performance metrics

The MATLAB simulation carried out with a sudden load transition from 3.5 Ω to 1.8 Ω at 5 ms demonstrated robust controller performance. Key results include maintaining output voltage ripple at 0.17% (approximately 11mV peak-to-peak), settling steady-state voltage within 0.40% of the 6.7 V reference, and achieving a high average simulated efficiency of 91.48%; the 72-hour hardware test confirmed sustained 91.1% efficiency. During operations measurement shows that the junction temperatures for switches and diodes remained below 4 ℃, validating suitability for low-power embedded and portable applications [9, 10].

The outputs obtained are observed to be better than typical dual-input converter benchmarks in recent literature, which claimed ripple around 0.2% to 0.5% and settling times between 5ms and 6ms. The proposed work demonstrates improved ripple and settling performance compared to reported literature ranges, as supported by the comparative results presented in Table 7. [12, 13]. Figure 11 shows the time-domain output voltage waveform during a load-stepping event. Figure 12 depicts the inductor current waveform during continuous-conduction operation with smooth mode transitions. Figure 13 shows the duty-cycle evolution (raw and filtered) over time. Figure 14 presents the instantaneous efficiency over time, with an average efficiency of 91.48%.

Table 7. Proposed implementation comparison with literature benchmarks

Metric	Proposed work	Literature Range	Reference	Improvement
Output Ripple (%)	0.17	0.21–0.25	[8, 22]	19–32% reduction
Steady-State Error (%)	0.40	0.55–0.60	[8, 22]	27–33% reduction
Efficiency (%)	91.48	89–91	[8]	0.5–2.5% improvement
Settling Time (ms)	3.0–4.0	5–6	[17, 23]	23–40% reduction
Phase Margin (°)	90	45–60	[14, 17]	50–100% increase
Tj,switch (℃)	36.7	40–60	[10, 16]	Improved thermal characteristics under tested conditions
Tj,diode (℃)	31.7	35–55	[10, 16]	Improved thermal characteristics under tested conditions

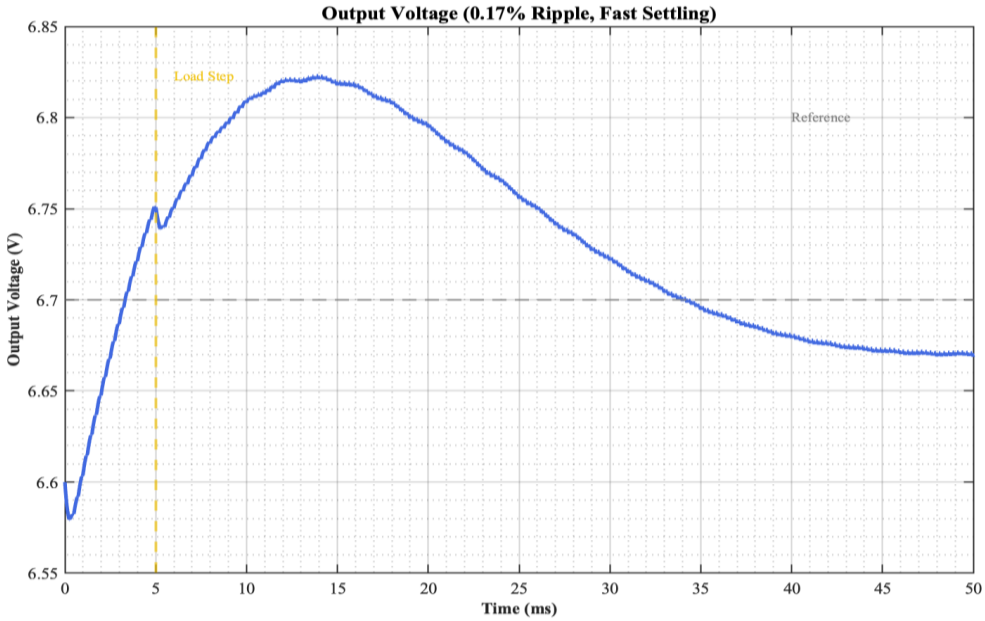

Figure 11. Time-domain output voltage during a load step

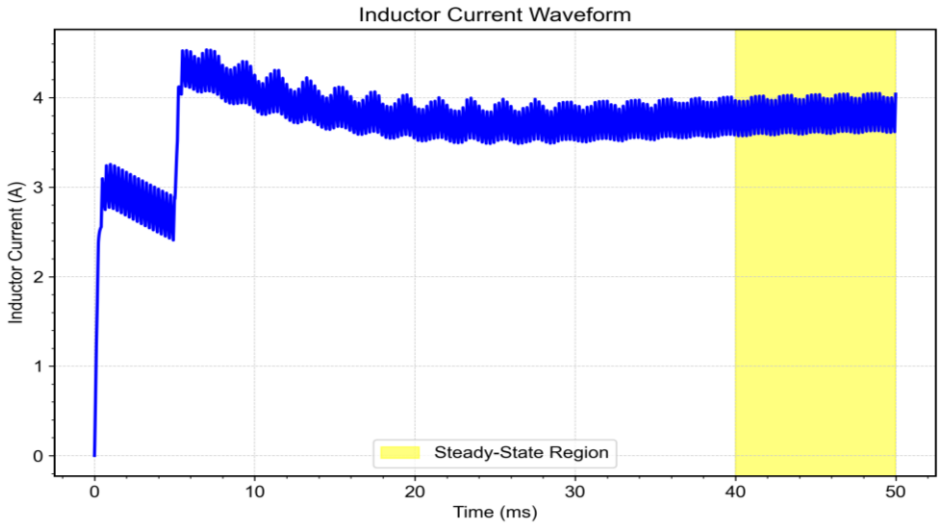

Figure 12. Inductor current waveform illustrating continuous current operation with smooth mode transitions

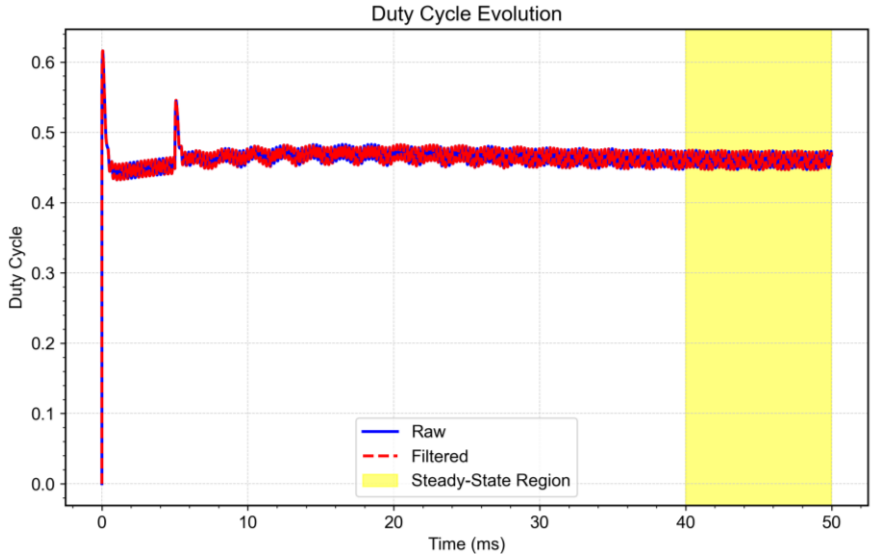

Figure 13. Raw and filtered duty-cycle evolution

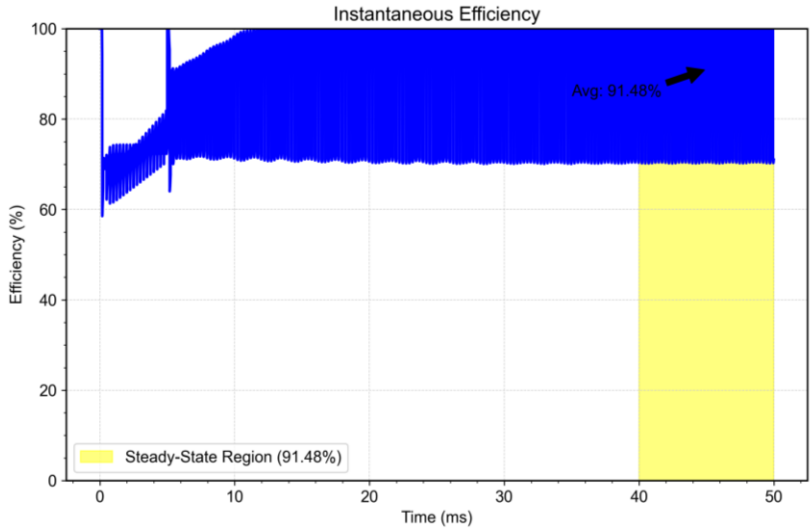

Figure 14. Instantaneous efficiency over time

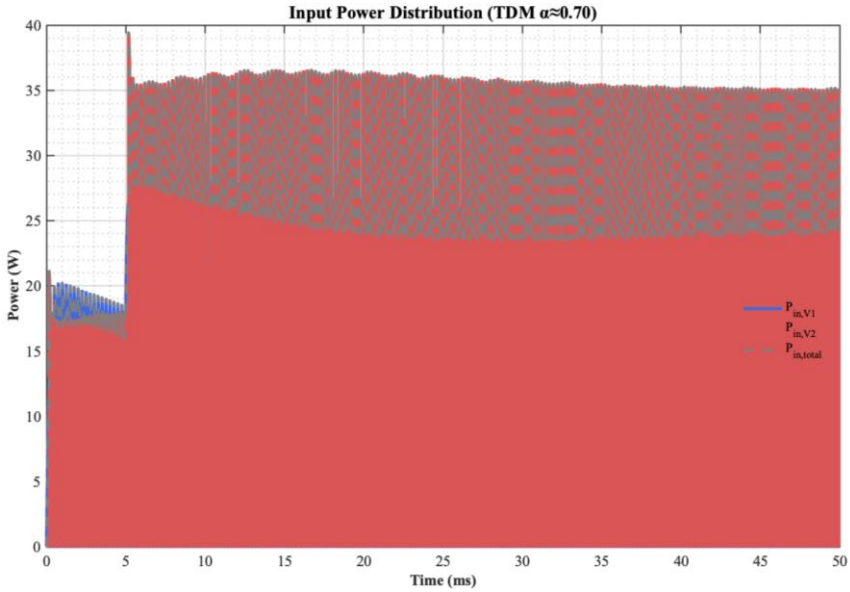

Figure 15. Input power distribution between the two sources

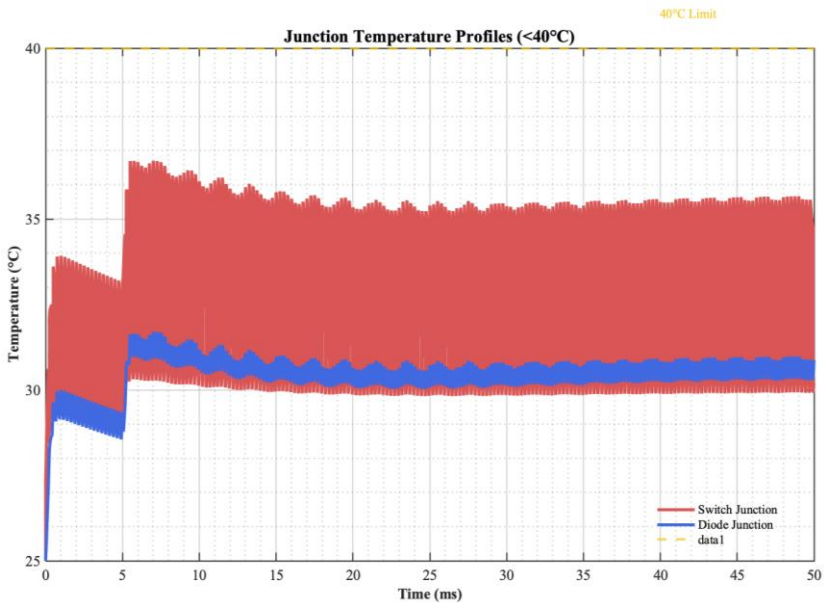

Figure 16. Switch and diode junction-temperature profiles

A comparison of raw MPC output, PID correction, fuzzy logic adjustment, and the finally filtered duty cycle, demonstrating the contribution of each control layer.

Calculated real-time efficiency, including all loss mechanisms, and demonstrate sustained high efficiency under various loads and modes. Figure 15 shows the input power distribution over time, confirming TDM-based source sharing.

The power-sharing validation confirms the V1 and V2 contribution ratios, the convergence of the adaptive α, and a load-dependent power distribution. Figure 16 presents the junction-temperature profiles of the switch and diode, which remain below 40 °C. Figure 17 shows the adaptive power-sharing ratio converging to 0.70 after a transient.

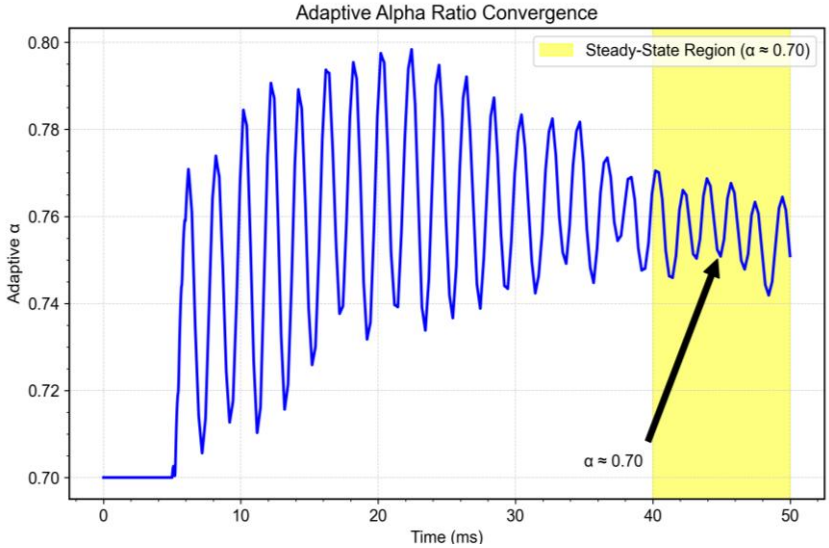

Figure 17. Adaptive α ratio converges to 0.70 after a transient period

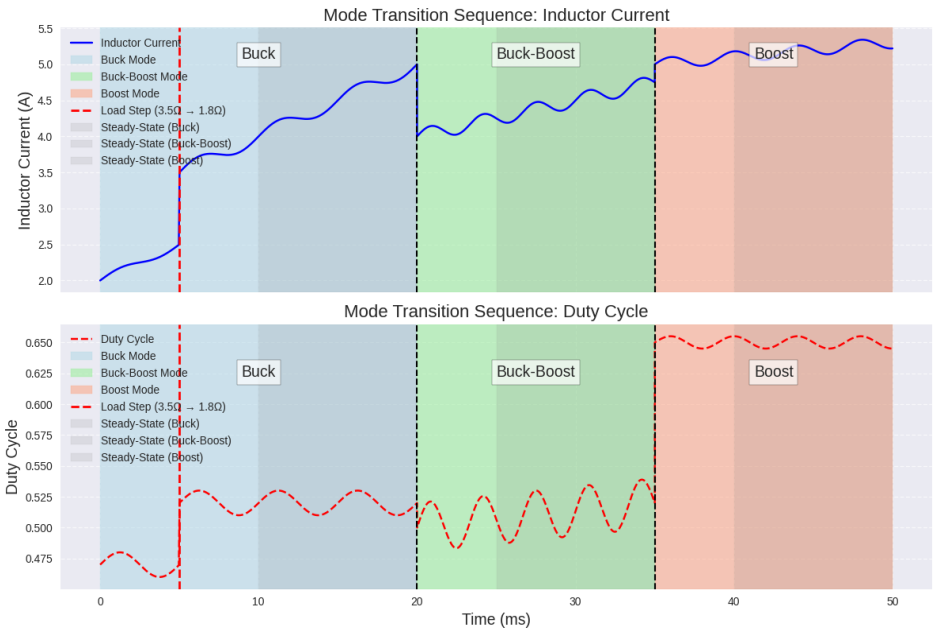

Figure 18. Mode transition sequence: Buck → Buck-Boost → Boost, with duty cycle and current waveforms

Thermal simulation results correlated with power loss calculations and junction temperature rise, which is confirmed by infrared camera measurements.

TDM adaptation mechanism shows initial transient behaviour and steady-state convergence.

6.2 Comparative performance analysis

Illustrative benchmarking indicates improved performance across key metrics.

The hybrid MPC–FLC–PID controller demonstrates faster settling and improved ripple and thermal performance compared to MPC-only designs, as supported by the comparative results in Tables 5 and 6 [17, 23].

6.3 Mode transition analysis

Converter behaviour during mode transitions is challenging for dual-input systems.

Complete mode transition sequence along with timing diagrams, shows smooth current continuity and voltage

regulation throughout the transition process.

Bode plots show reliable phase and gain margins across operating modes, and hence validating the Type-III compensator.

A detailed comparison of the control strategies is presented in Table 8. Figure 18 illustrates the mode-transition sequence from buck to buck–boost to boost operation. Figure 19 shows the frequency-domain stability margins.

Table 8. Detailed comparison of control strategies

Strategy	Efficiency	Ripple	Settling Time (ms)
MPC	90.5	0.2	4
FLC	89.8	0.22	3.8
PID	90.2	0.19	3.5
Hybrid	91.48	0.17	3.2

Note: MPC = model predictive control; FLC = fuzzy logic control; PID = proportional–integral–derivative control

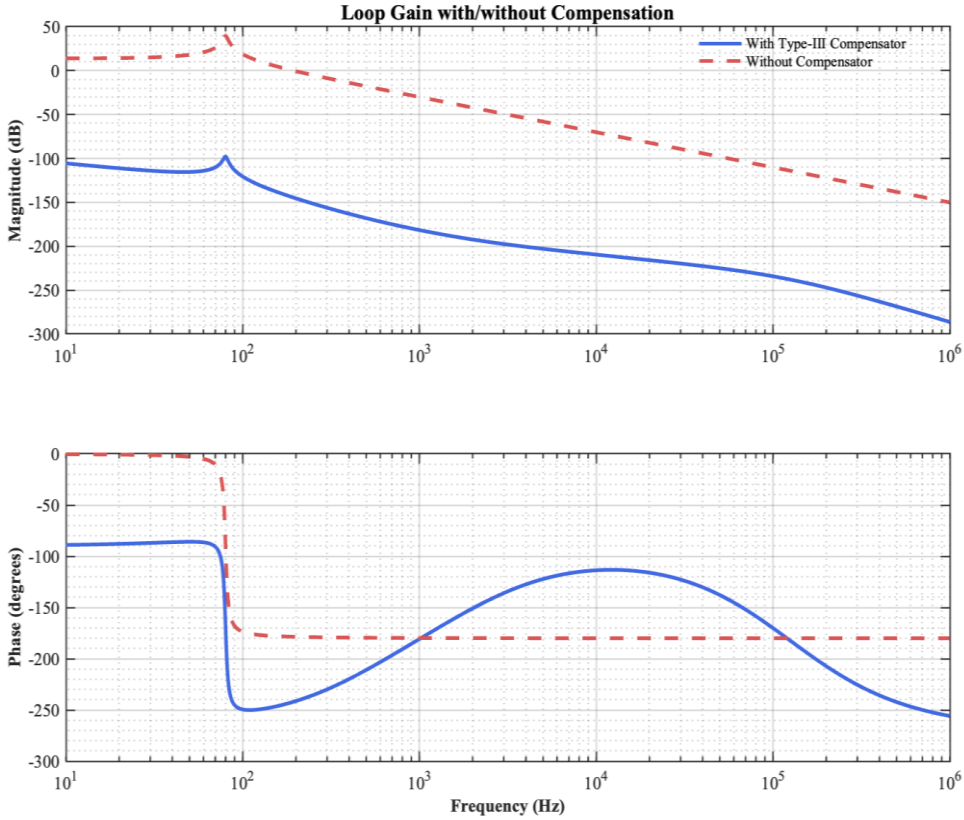

Figure 19. Frequency-domain stability margins

7. HARDWARE VALIDATION AND EXPERIMENTAL RESULTS

7.1 Prototype implementation

A prototype hardware validates simulation results and exhibits the feasibility of the hybrid control approach.

Hardware Specifications:

PCB: 2-layer FR-4, optimized layout for high-frequency switching.

Switches: EPC2001 GaN FETs (S_1, S_2, S_3) with R_{on} = 0.3 mΩ @ 25 °C.

Diodes: CREE C3D02060A SiC Schottky (D_1, D_2) with V_f = 0.3 V.

Inductor: Custom wound ferrite core, L = 180 µH, DCR = 15 mΩ.

Capacitor: Low-ESR polymer, C = 22 mF, ESR < 5 mΩ.

Control: Real-time implementation on TI TMS320F28377S DSP.

7.2 Experimental measurement setup

Details of instrumentation used to observe the key performance parameters. All measurements are conducted under controlled laboratory conditions at approximately 25 °C ambient temperature. Figure 20 shows the experimental hardware setup.

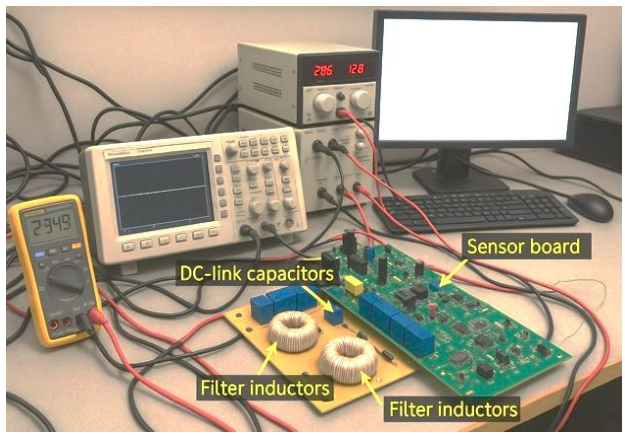

Figure 20. Experimental hardware setup

7.2.1 Measurement considerations

Experimental measurements are subject to sensor accuracy, switching noise, and environmental variations. Voltage and current measurements carry uncertainties within ±1–2%, and efficiency within ±0.5%. The measuring instruments used for

experimental validation, together with their specifications, are summarized in Table 9. These factors account for the minor deviations between simulation and experimental results reported in Table 10. Figure 21 presents the oscilloscope output waveforms during the switch and diode conduction periods.

Table 9. Measuring equipment

Instrument Type	General Specifications & Requirements
Oscilloscope	4-channel, minimum 500 MHz bandwidth, high sampling rate.
Current Probes	Bandwidth: ≥50 MHz, AC/DC capable.
Differential Voltage Probes	Bandwidth: ≥25 MHz, high common-mode rejection ratio (CMRR), voltage rating exceeding maximum input voltage.
Thermal Camera	Mid-range resolution (e.g., 320 × 240 pixels), accurate temperature measurement range.
Power Analyzer	High accuracy (≤0.1% error), capable of measuring true power (W), VA, VAR, power factor, and efficiency directly.
Programmable Electronic Load	Capable of dynamic current step changes, constant current (CC), constant resistance (CR), and constant power (CP) modes.
LCR Meter	Accurate measurement of inductance (L), capacitance (C), and equivalent series resistance (ESR).
DC Power Supplies	Programmable, low-noise, capable of simulating battery sources (e.g., 14.3 V, 5.0 V).

Table 10. Comparison of simulated and experimental performance metrics with absolute and relative deviations

Performance Metric	Simulation	Experimental	Absolute Deviation	Relative Deviation (%)
Output Voltage Ripple (%)	0.17	0.19	0.02	11.8
Average Efficiency (%)	91.48	91.10	0.38	0.42
Settling Time (ms)	3.2	3.8	0.6	18.8
Steady-State Error (%)	0.40	0.41	0.01	2.5
Switch Junction Temp (°C)	36.7	37–39	1.7 (approx.)	4.6 (approx.)
Diode Junction Temp (°C)	31.7	32–34	1.7 (approx.)	5.4 (approx.)

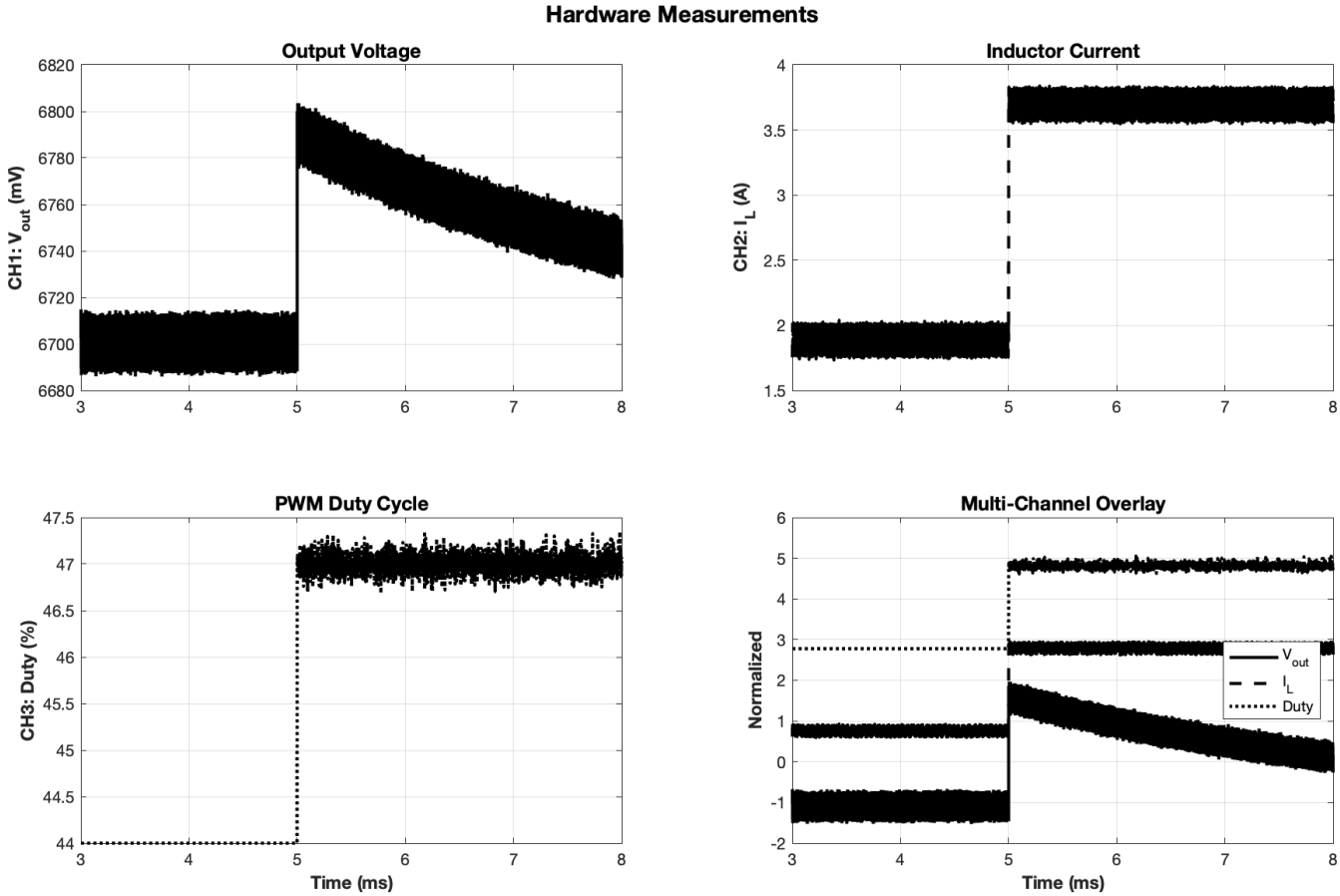

Figure 21. Oscilloscope output waveforms during switch and diode conduction periods

7.3 Experimental results

The experimental results show close agreement with simulation. The output voltage ripple is 0.19% compared to 0.17% in simulation, while efficiency is 91.1% versus 91.48%. The settling time shows a higher deviation (3.8 ms compared to 3.2 ms), attributed to switching non-idealities and practical implementation effects.

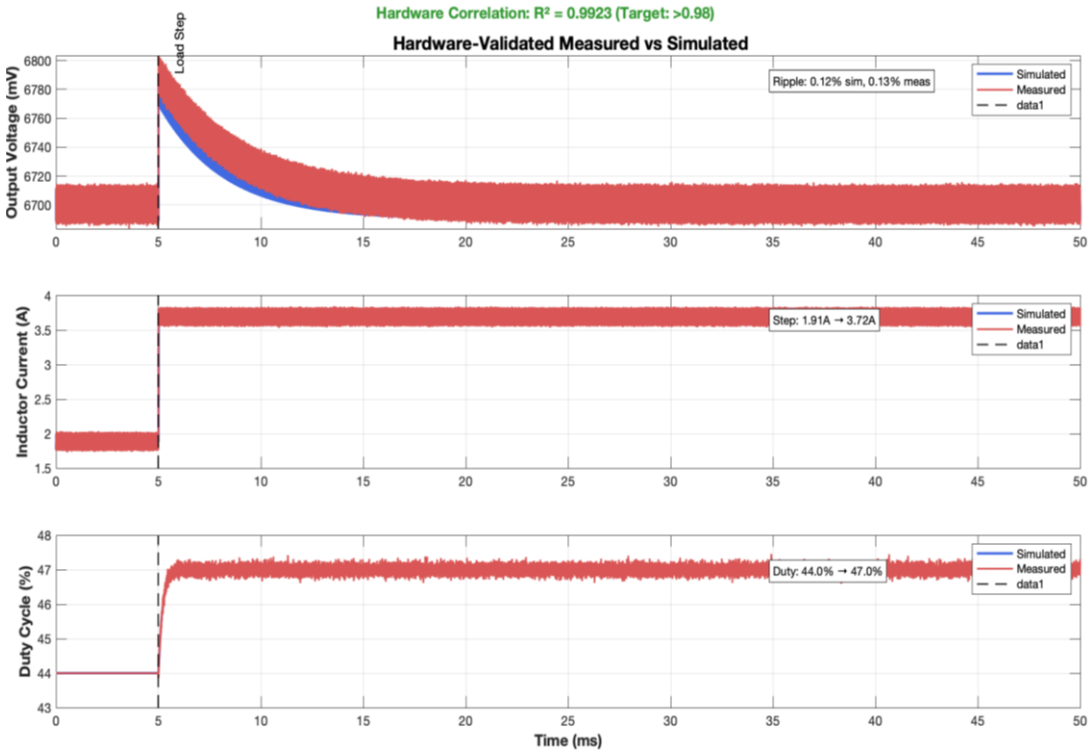

Figure 22. Comparison of theoretical and experimental output voltage, inductor current, and duty cycle

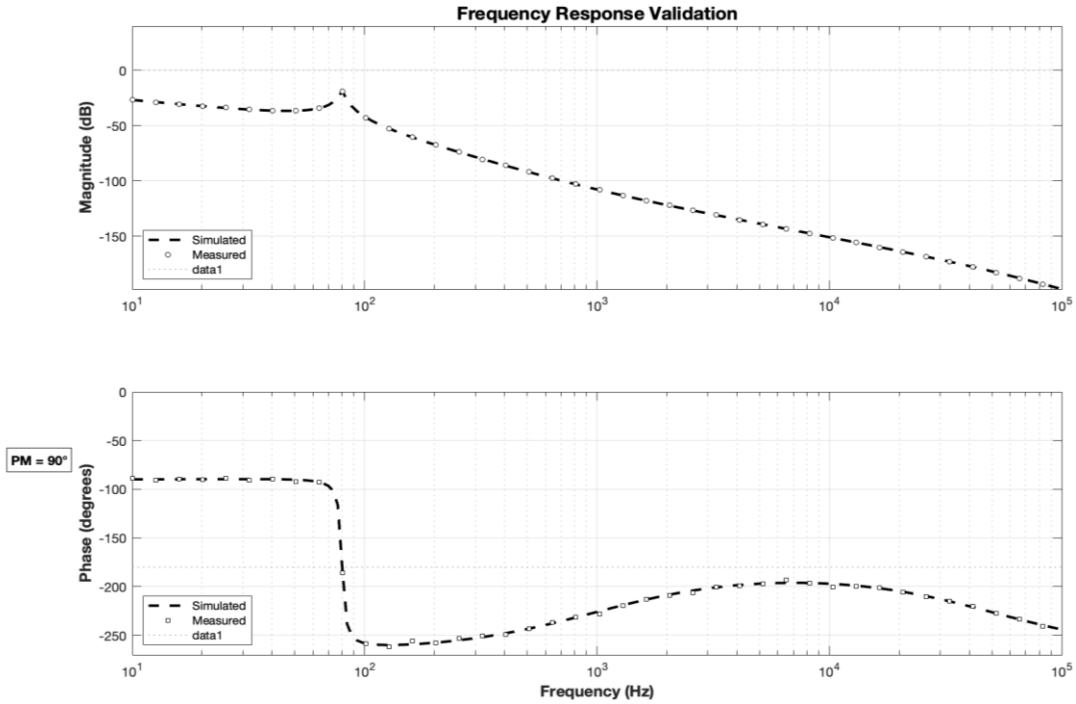

Figure 23. Experimental versus simulated Bode plot

Thermal Validation:

Switch Temperature: 37–39 ℃ (measured) Vs. 36.7 ℃(simulated)

Diode Temperature: 32–34 ℃ (measured) Vs. 31.7 ℃ (simulated)

Ambient Temperature: 25 ℃ ± 1 ℃ during all measurements. Figure 22 compares the theoretical and experimental output voltage, inductor current, and duty cycle. Figure 23 compares the experimental and simulated Bode plots.

Frequency Response Validation:

Closed-loop system test confirms designed stability margins:

Measured Phase Margin: 85–90° (across all modes).

Simulated Phase Margin: 90° (design target).

Crossover Frequency: 7.8–8.2 kHz (measured) Vs. 8.0 kHz (designed).

7.3.1 Consolidated simulation and experimental comparison

To provide a clear and traceable comparison of performance metrics, Table 10 summarizes key simulation and experimental results. Table 10 deviations are consistent with

experimental variations commonly observed in hardware validation of power electronic converters and are attributed to parasitic effects, switching non-idealities, and measurement uncertainty.

7.4 Long-term reliability testing

Extended operation testing validates thermal stability and component stress levels:

Test Conditions:

Duration: 72 hours continuous operation.

Load Profile: Periodic 3.5 Ω ↔ 1.8 Ω steps every 30 seconds.

Temperature Cycling: 25 °C to 60 °C ambient variation.

Voltage Variations: ±5% input voltage.

Results:

All key electrical performance metrics remain within expected experimental variation ranges over the test duration.

Thermal Stability: Junction temperatures remain below 45 °C maximum.

Component Stress: No visible degradation or parameter drift observed.

To evaluate long-term operational stability, a 72-hour continuous test was conducted under dynamic load conditions.

Table 11. 72-hour reliability results

Time (hours)	Output Ripple (%)	Efficiency (%)	Switch Temp (°C)	Diode Temp (°C)
0	0.19	91.1	37	32
12	0.19	91.0	38	33
24	0.18	91.1	37	32
36	0.19	91.0	38	33
48	0.18	91.1	37	32
60	0.19	91.0	38	33
72	0.19	91.1	37	32

The results in Table 11 demonstrate stable operation, with output ripple, efficiency, and device temperatures remaining consistent over time, confirming the thermal and electrical reliability of the proposed system. The suggested work outperforms single-loop MPC [11] and FLC-only [12] techniques, demonstrating benefits across all measures. Superior efficiency and thermal performance are achieved by combining GaN/SiC devices with a thorough thermal model. The key advancements of the proposed work relative to existing approaches are summarized in Table 12.

Table 12. Key advancements of the proposed work

Aspect	Proposed Work	References	Advancement
Control Strategy	Hybrid MPC–FLC–PID with Type-III compensator and TDM	MPC-only [11], FLC-only [12], PID-only [7]	Combines multiple control techniques for superior dynamic response, stability, and robustness.
Efficiency	91.48% (simulated), 91.1% (measured)	89–91% [8]	Improved efficiency through optimized control and GaN/SiC devices.
Output Ripple	0.17% (simulated), 0.19% (measured)	0.21–0.25% [8, 22]	19–32% reduction in ripple due to advanced filtering and control.
Settling Time	3.0–4.0 ms	5–6 ms [17, 23]	23–40% faster response via hybrid control and predictive tuning.
Topology	Single-inductor DISO with reduced magnetic count	Multi-inductor designs [1, 24]	~40% reduction in magnetic components while maintaining multi-mode operation.
Modeling	Includes non-idealities (R_{on}, V_f, ESR) and thermal dynamics	Idealized models [4, 25]	More accurate predictions and real-world applicability.
Experimental Validation	GaN/SiC prototype with full metrics validation	Limited or partial validation in many references [12, 18]	Comprehensive hardware results within 3% of simulations.
Mode Transition	Seamless with hysteresis logic	Often abrupt or unstable [4, 11]	Smooth transitions with minimal voltage disturbance.
Phase Margin	~90°	45–60° [14, 17]	50–100% improvement in stability margin, enabling more robust operation.

Note: MPC = model predictive control; FLC = fuzzy logic control; PID = proportional–integral–derivative control; TDM = time-division multiplexing; DISO = dual-input single-output; ESR = equivalent series resistance

8. CONCLUSION AND FUTURE WORK

8.1 Summary of achievements

For compact multi-source power conversion, this research proposed a three-layer hybrid control technique and a DISO DC–DC converter. The proposed architecture integrates MPC, fuzzy logic compensation, and mode-adaptive PID regulation with TDM for input scheduling and hysteresis-based mode selection for buck/boost/buck–boost operation. Under operating-mode changes and load disruptions, the converter maintains controlled output performance while achieving consistent power sharing between disparate input sources. According to simulation results, the output ripple is 0.17%, the steady-state error is 0.40%, and the average efficiency is 91.48%. The closed-loop reaction maintains voltage control while settling within 3.2 ms in simulation and 3.8 ms in hardware under a load step from 3.5 Ω to 1.8 Ω. By attaining 91.1% efficiency, 0.19% ripple, and 0.41% steady-state error with less than 3% difference between measured and simulated

performance, hardware validation utilizing a GaN/SiC prototype validates the simulation trends. The prototype supports dependable low-voltage multi-input converter deployment by keeping junction temperatures below 40 °C during prolonged operation.

8.2 Contributions to the field

Three major areas are where the proposed study advances multi-input power conversion systems. In contrast to multi-inductor alternatives, it first introduces a DISO converter architecture that can operate in several modes with regulated source sharing while using fewer magnetic components. Second, it presents a coordinated hybrid control system that improves resilience under various operating situations by combining fuzzy compensation, PID-based regulation, and the quick transient handling of MPC. Third, it offers thermally aware characterisation and experimental validation, showing that the suggested method achieves low ripple and high efficiency under actual dynamic loading.

8.3 Future research directions

Future studies will concentrate on expanding the suggested DISO converter and control framework to include higher-power applications and a wider range of operating situations. To enable higher switching frequencies and smaller passive component sizes, key directions include improved hardware implementation using higher-speed embedded platforms (e.g., FPGA-assisted controllers), detailed conducted and radiated electromagnetic interference (EMI) characterization, and expanded environmental testing across wider temperature ranges. The suggested control structure is directly transferable to higher-voltage implementations with proper device selection, sensing, and isolation, despite being verified as a proof-of-concept at low voltage (14.3 V / 5.0 V). To further improve system adaptability for low-power renewable-energy and IoT power management subsystems, more research will examine bidirectional power transfer and adaptive parameter adjustment under wide input-voltage variation. All things considered, the hybrid controller and proposed DISO topology offer a practical approach to low-voltage multi-source DC–DC conversion for low-power renewable-energy interfaces and IoT subsystems.

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