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Design a 27-Level Cascaded H-Bridge Inverter Using ONE DC Voltage Source

Laith A. Mohammed[1*], Rakan Khalil Antar[1], Basil M. Saied[2]

[1] Electrical Engineering Techniques, Northern Technical University, Mosul 41001, Iraq
[2] Electrical Engineering, Mosul University, Mosul 41001, Iraq

Corresponding Author Email: laith.akram@ntu.edu.iq

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ABSTRACT

Multilevel cascaded H-bridge inverter with unequal DC voltage sources (DCVS) is used to reduce distortions and get different output voltages higher than conventional type. In addition, to avoid the complexity of using multi-DC power sources, a single DCVS is utilized to obtain a 27-level cascaded H-bridge inverter that is implemented in this study. The one input DCVS of the H-bridge inverter, which may be fed from solar cells, is divided into three unequal values. The ONE DCVS is fed to a single-phase H-bridge inverter and the output is connected to transformer with three windings. The transformer's outputs fed two single-phase uncontrolled rectifiers to get 1/3Vdc and 1/9Vdc values, which have been used as DC inputs for two cells of the cascaded H-bridge inverter, and the third cell is fed from the ONE DCVS. The system is built and executed by MATLAB program and an embedded S-function. The designed system based on ONE DCVS is built with a structure of (1:1/3:1/9) Vdc to get a 27-level output voltage. Simulation results prove that the 27-level output voltage is produced using ONE DCVS. The THD values of the output voltage and current at power factor 0.8 are 1.1624% and 0.1838%, while they are, respectively, equal to 1.496% and 0.1334% at power factor 0.5. The efficiency values of the system are 99.7254% and 98.9785% at power factors of 0.8 and 0.5, respectively. Also, the system is built to get instantaneously variable output levels from 7-level to 27-level with acceptable THD.

1. INTRODUCTION

Power DC/AC converter structures are considered to give an AC voltage from a DC voltage source (DCVS). An inverter is supposed to offer continuous and ripple-free, as close as possible to the ideal AC voltages with low total harmonic distortion (THD) to ensure the equipment's safety. Medium-voltage and high-power applications have required using multilevel power converters. One essential key of voltage source inverters is power quality. Pure sine waves are preferred to be produced by voltage source inverters, but this isn't always feasible, especially in real-world applications [1]. To get good power quality, a high switching frequency with two-level inverters is required, which reduces conversion efficiencies [2]. Conversely, multilevel inverters lead to decreasing in cost and THD and improve efficiency [3]. Multilevel voltage source inverters have more advantages than conventional pulse width modulation (PWM) voltage source inverters in higher power applications. The general structure of the multilevel voltage source inverter (MLVSI) is to produce a sinusoidal voltage by combining multiple voltage levels [4]. So, it has become an active and useful key for decreasing switching losses in industrial applications [5]. Also, the synthesized output voltage adds more steps as the number of voltage levels on the DC side increases to produce output voltage as sinusoidal a wave as possible with minimum THD. As highlighted in references [6-9], an MLVSI plays an essential role in changing power for connecting power systems and different low-voltage applications. The diode-clamped, flying capacitors, and cascaded multilevel inverters are the multilevel topologies. The number of DC sources, capacitors, switches, diodes, and clamped capacitors are listed in Table 1. The cascaded multilevel inverters have more advantages than the other two types, while their disadvantages are requiring one isolated DCVS for each cell [10]. The THD of the outputs reduces as the number of output voltage increases. Equal DCVSs of the MLVSI are used in the first development. In order to reduce the THD of the MLVSI outputs, unequal DCVSs are also used. The unequal DCVSs of each inverter cell have unequal DC voltages, unlike the equal DC voltages to control the output voltage level. Different control techniques are used to improve the MLVSI's performance, such as sinusoidal PWM, space-vector PWM, selective harmonics elimination, model predictive control, nearest-level control, genetic algorithm, and the anti-predatory particle swarm optimization technique [11-15].

In recent years, various researchers have reported the use of the cascaded H-bridge multilevel voltage source inverter (CHMLVSI) in both static and drive applications. The CHBMLVSI with unequal DCVSs (27-level) is designed and used by Raj and Nair [16] and Vasanthakumar and Nafeena [17] depending on different driving strategies with THD of the output phase voltage waveform equal to 6.28% and 3.06%, respectively. A one-source, five-level switched capacitor

MLVSI was presented by Siddique and Mekhilef [18] with fewer components and a lower value of THD.

Table 1. Comparisons of component per leg of MLI converters

Type of MLVSI	Diode Clamped	Flying Capacitor	Cascaded H-Bridge
DC source	1	1	(L-1)/2
DC capacitor	L−1	L−1	-
switch	2(L−1)	2(L−1)	2(L−1)
clamped capacitor	0	(L−1)*(L-2)/2	0
clamped diodes	(L−1)*(L-2)	0	0

L is the number of levels.

An MLSVI suggested by Jena et al. [19] with two switched capacitors and ONE DC source was modelled to reduce overall component and cost. The designed system produces 7-level output voltage. The important thing is boosting ability that does not require the need to boosting voltages, especially by using renewable sources. In 2022, Dhanamjayulu et al. [20] built a 35-level inverter using five DC sources and ten unidirectional and bidirectional switches. This circuit is used in low- to medium-power applications, especially battery systems where isolated DC sources exist. A series and parallel connection of single-source and double-source was proposed by Wang et al. [21] to form multilevel output. This topology can cause a short circuit of DC sources while connecting the sources with high voltage stresses between switches.

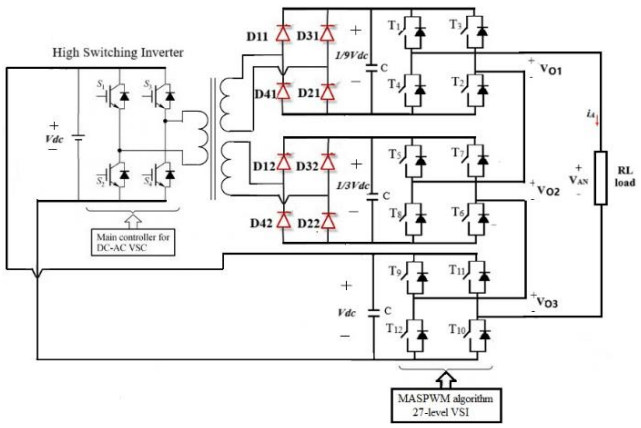


Figure 1. The proposed single-phase CHMLVSI fed from ONE DC source

According to what reviewed above, in addition to the drawbacks of using multiple isolated DC sources compared with using a single output of a DC source to feed a multi-level H-bridge inverter which increase complexity due to needing more safety for secure isolations as a result increased weight, size, cost, control elements, and power losses, this paper presents a single-phase, three-cell CHMLVSI fed from ONE DC source to get 27-level output voltages. The DC source, which may be a PV system, is fed to a single-phase inverter, and the output is an input to a single-phase transformer with two-output of transformation ratio of (1:1/3, 1:1/9). The next step is two single-phase rectifiers to get (1/3) Vdc and (1/9) Vdc. These DC voltages are used as inputs of the CHMLVSI as shown in Figure 1. The controller is built using the modified absolute sinusoidal pulse width modulation (MASPWM) algorithm used in references [22-24]. The system can be designed with single-input three-winding output transformer to consider full isolation for protection purposes, but the size, cost, weight, losses, and interference problems will increase. For this reason, single-input two-winding output transformer is selected. Unlike the cascaded H-bridge inverters in references [16, 17] which require multiple isolated DC sources, the key innovations of the proposed topology utilize a single power source configuration. Furthermore, it differentiates the proposed MASPWM control strategy from the modulation techniques used in references [18-21], emphasizing the benefits of lower THD and simplified control logic.

2. TWENTY-SEVEN LEVEL CASCADED H-BRIDGE INVERTER

The multilevel inverter allows its output to reach a smoothly high voltage with low harmonics. The level capacity can be improved by replacing the equal DCVSs with unequal different values of input DC voltages for each H-bridge cell. The contribution of this study is to get different AC voltage levels with minimum THD values depending on ONE DCVS. The ONE DCVS gets from a battery or solar cell is divided into three unequal isolated values. It is fed to a single-phase DC/AC high-switching inverter and the output is connected to a single-phase, three-winding, high frequency power, transformer as shown in Figure 1. The transformer outputs fed two single-phase uncontrolled AC/DC rectifiers to achieve 1/3Vdc and 1/9Vdc values with the ONE DC voltage (V_{dc}) as inputs for the three H-bridge inverter cells. The output voltages of each inverter cell (V_{O1}, V_{O2}, and V_{O3}) produce the wanted output voltage (V_{AN}) of the designed MLVSI:

$$V_{AN} = V_{O1} + V_{O2} + V_{O3} \quad (1)$$

In general, the amount of THD in percent is defined as:

$$THD\% = \frac{\sqrt{\sum_{h=3,5,7,..}^{\infty} I_h^2}}{I_1} \quad (2)$$

where, I_h and I_1 are the harmonic and fundamental components of the output inverter current, respectively. The procedures for producing different isolated DC sources from an OND DC source is given in the flowchart illustrated in Figure 2.

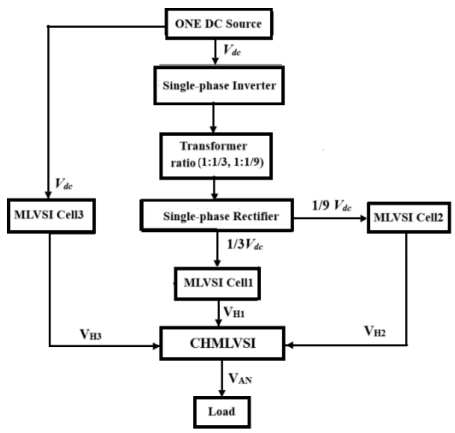


Figure 2. Flowchart of producing different isolated DC sources from ONE DC source

3. CONTROL STRATEGIES

In MLVSI applications, specific numbers of PWM strategies are used. The PWM strategies can be categorized into fundamental frequency switching modulation strategy, space-vector PWM strategy, and carrier based PWM strategy, which has one-carrier or more [10]. In this paper, a MASPWM method proposed by the studies [22-24] is adopted using a triangular as a carrier signal. The controller circuit employs a single-carrier approach. The proposed controller technique operates by generating an absolute sinusoidal reference that defines the target voltage amplitude. Figure 3 shows the flowchart of the MASPWM controller that tracks the zero-crossing points of this reference to create a corresponding discrete, quantized signal. The core modulation signal is then derived by subtracting this quantized sequence from the original absolute reference; this difference is what is compared against the single triangular carrier to generate the PWM pulses. To execute this, a custom MATLAB S-function controls the logic, distributing firing pulses to the IGBTs based on specific switching states illustrated in Table 2. This control scheme can successfully synthesize output voltage levels from 3-level to 27-level. Different output voltage levels can be obtained based on the DCVS values that feed the CHMLVSI. Therefore, due to unequal DCVS of each inverter cell (Vdc, 1/3Vdc, and 1/9Vdc), thirteen level appears in the positive side and thirteen level in the negative side with zero level to get 27-level output voltage as clarified in Table 2.

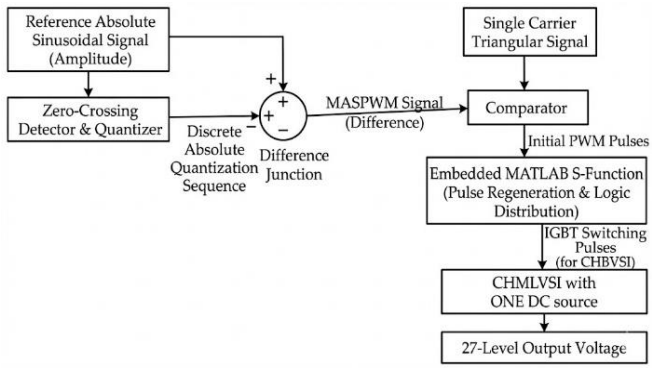


Figure 3. Flowchart of the single-carrier MASPWM control strategy for a 27-Level single-source CHMLVSI

Table 2. Switching state patterns of the output phase voltage levels of a single-phase CHMLVSI

Cell 1				Cell 2				Cell 3				V_{AN}
T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	
0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	1	0	1	0	1	0	1	Vdc/9
0	0	1	1	1	1	0	0	0	1	0	1	2Vdc/9
0	1	0	1	1	1	0	0	0	1	0	1	Vdc/3
1	1	0	0	1	1	0	0	0	1	0	1	4Vdc/9
0	0	1	1	0	0	1	1	1	1	0	0	5Vdc/9
0	1	0	1	0	0	1	1	1	1	0	0	6Vdc/9
1	1	0	0	0	0	1	1	1	1	0	0	7Vdc/9
0	0	1	1	0	1	0	1	1	1	0	0	8Vdc/9
0	1	0	1	0	1	0	1	1	1	0	0	Vdc
1	1	0	0	1	0	1	0	1	1	0	0	10Vdc/9
0	0	1	1	1	1	0	0	1	1	0	0	11Vdc/9
1	0	1	0	1	1	0	0	1	1	0	0	12Vdc/9
1	1	0	0	1	1	0	0	1	1	0	0	13Vdc/9

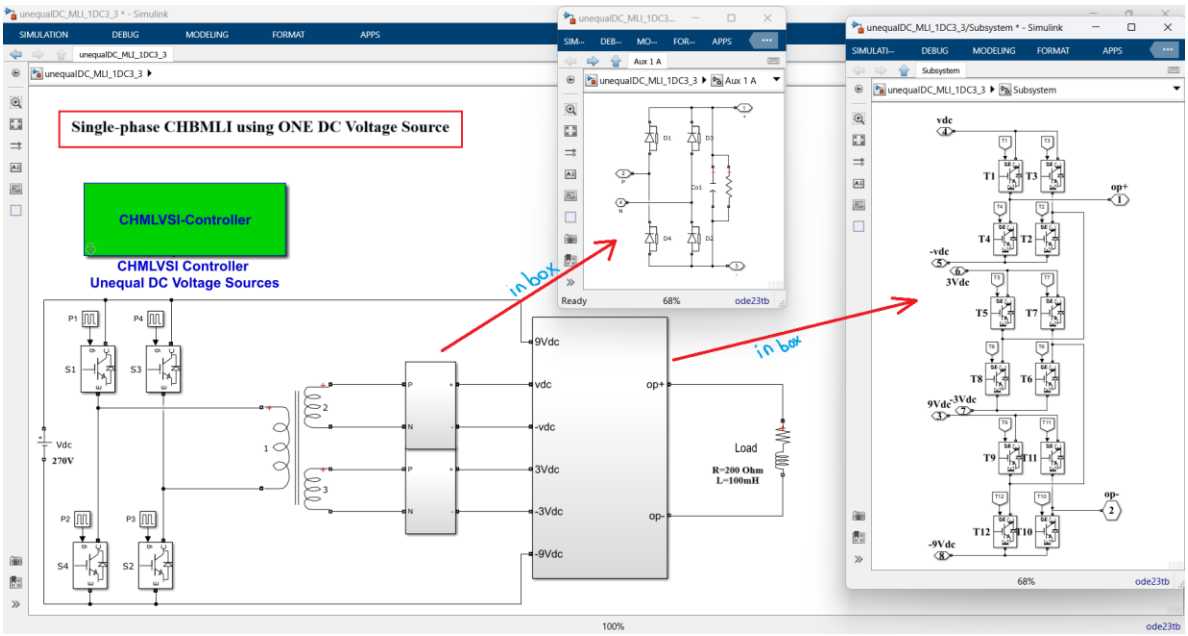
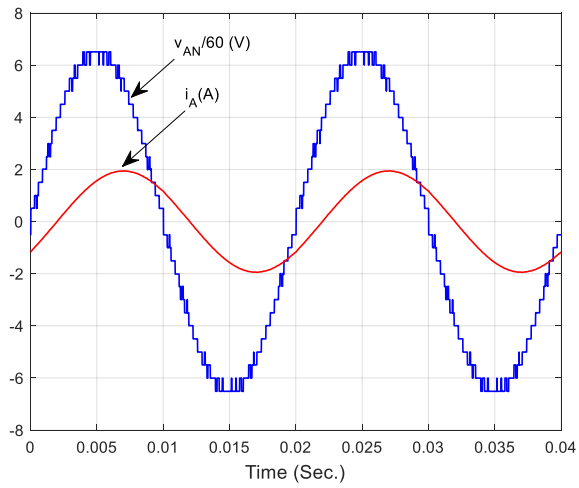


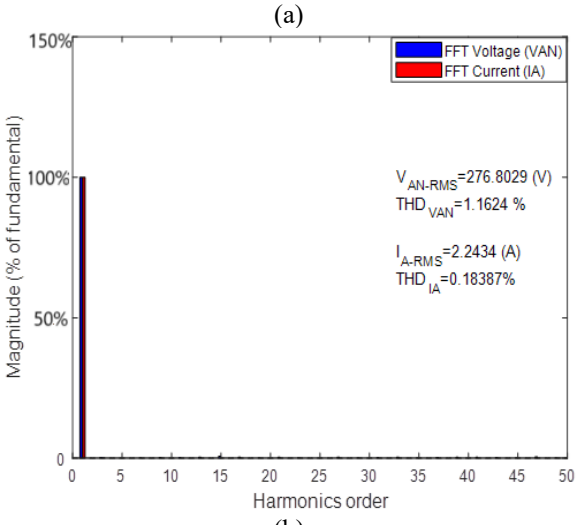
Figure 4. The proposed single-phase CHMLVSI fed from ONE DC source

4. SIMULATION RESULTS

Depending on the needed industrial application, the output voltage levels of the CHMLVSI change using unequal DCVSs. The ONE DCVS is selected equal to 270V, which is chosen to match a specific load requirement (like a motor). The switching frequency of the single-phase bridge inverter and CHMLVSI is chosen to be equal to 50 Hz and 1 kHz, respectively. The main justification for using a 27-level inverter is that the high number of voltage steps creates a smooth sine wave naturally. This means it does not need a high switching frequency like 10kHz or 20kHz to get good power quality. So that, choosing 1kHz minimizes switching losses (heat) and improves efficiency without sacrificing THD. The single-phase two-winding output linear transformer with 50Hz is selected with voltage transformation ratio of 270/90/30V. The designed modelling circuit is illustrated in Figure 4. The modelling results of the output voltage (V_{AN}) and current (I_A) with their spectrum analyzer of the twenty-seven levels CHMLVSI presented for different RL loads are shown in Figure 5 and Figure 6. The modeling study proves that the THD values with zero level in the output voltages are higher than without zero level, so that the outputs are designed and modeled without zero-level. The THD of the output voltage and current at a power factor of 0.5 is 1.496% and 0.1334%, respectively. While at a power factor of 0.8 lagging, the THD are 1.1624% and 0.18387%, respectively. The results show that the proposed 27-level inverter yields a voltage THD of 1.1624%–1.496%, which is superior to the 6.28% [16] and 3.06% [17].



(a)



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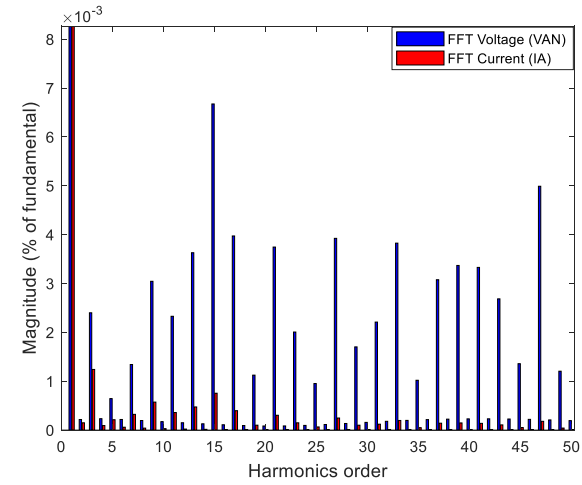
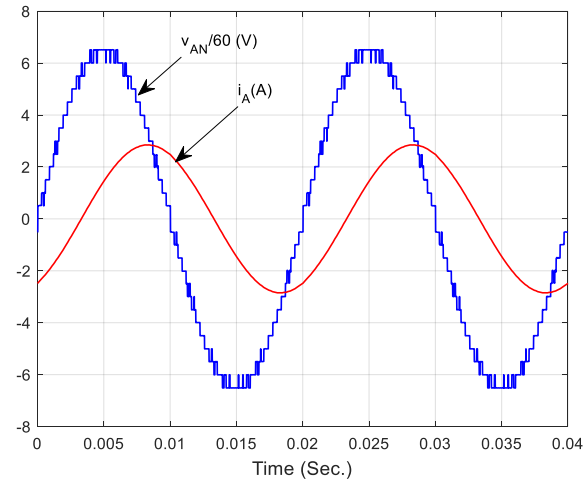


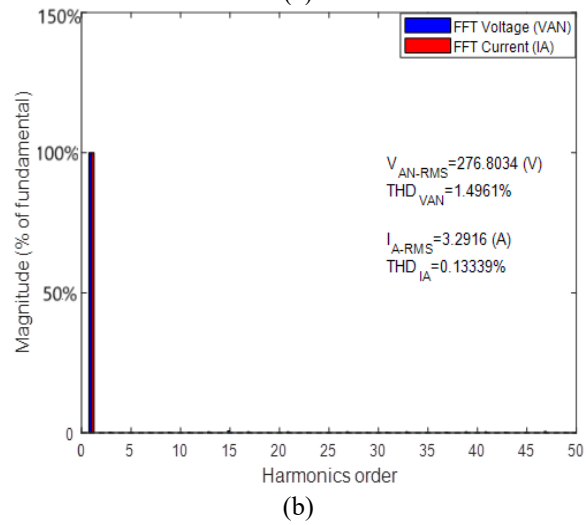
(c)

Figure 5. The 27-level (a) output voltage and current with their (b) spectrum analyzer at PF = 0.8 and (c) zoom section for the low harmonics order

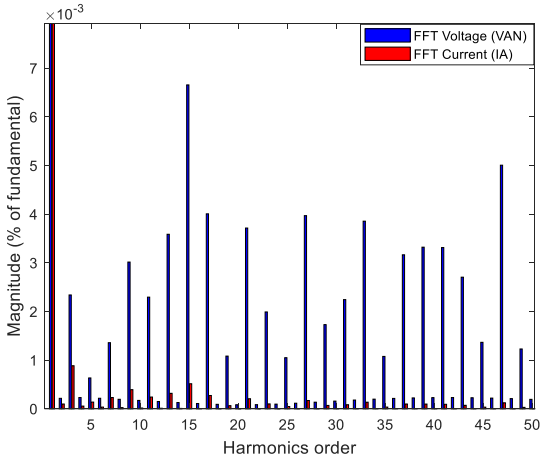
This reduction confirms the superiority of the MASPWM technique in synthesizing a high-quality sinusoidal waveform. The amplitude of the low harmonic orders shown in Figure 5(c) and Figure 6(c) is around zero with insignificant values of the higher harmonic orders. The whole system's efficiency is 99.7254% at a power factor of 0.8 and 98.9785% at a power factor of 0.5. The efficiency was derived directly from the simulation environment by monitoring the instantaneous input and output power.



(a)



(b)



(c)

Figure 6. The 27-level (a) output voltage and current with their (b) spectrum analyzer at PF = 0.5 and (c) zoom section for the low harmonics order

The average output power (P_{out}) delivered to the load and the total input power (P_{in}) drawn from the DC source were calculated over steady-state cycles. The efficiency (η) was then computed using the standard formula:

$$\eta = \frac{P_{out}}{P_{in}} \tag{3}$$

The steady state and dynamic waveforms of the V_{AN} at levels from 15 to 27 are illustrated in Figure 7. Specifically, the figure shows the transition from 15-level operation to 27-level operation (changing the reference voltage amplitude). This confirms the controller's ability to track sudden changes in the reference signal without instability. The THD values of the V_{AN} and I_A at different voltage levels with different RL loads are illustrated in Figure 8. To verify these results, the apparent, real, reactive, and distortion power components are taken into account at various levels as explained in Figure 9. These power waveforms explained the effect of increasing loads and voltage levels on the amount of power levels.

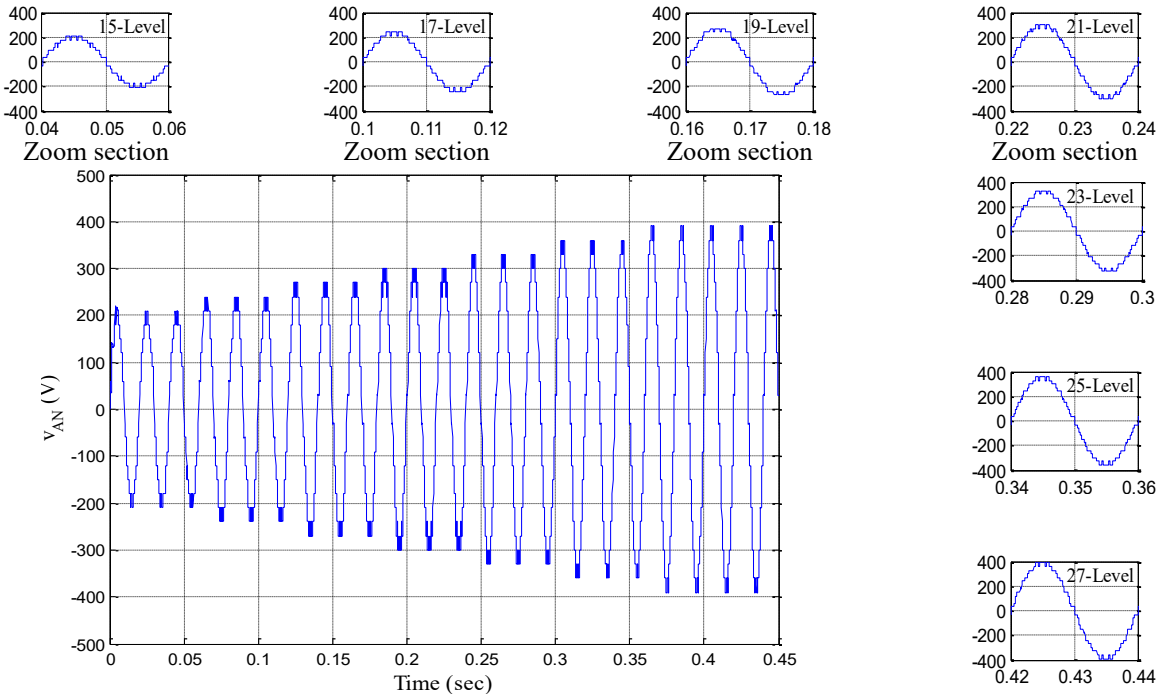
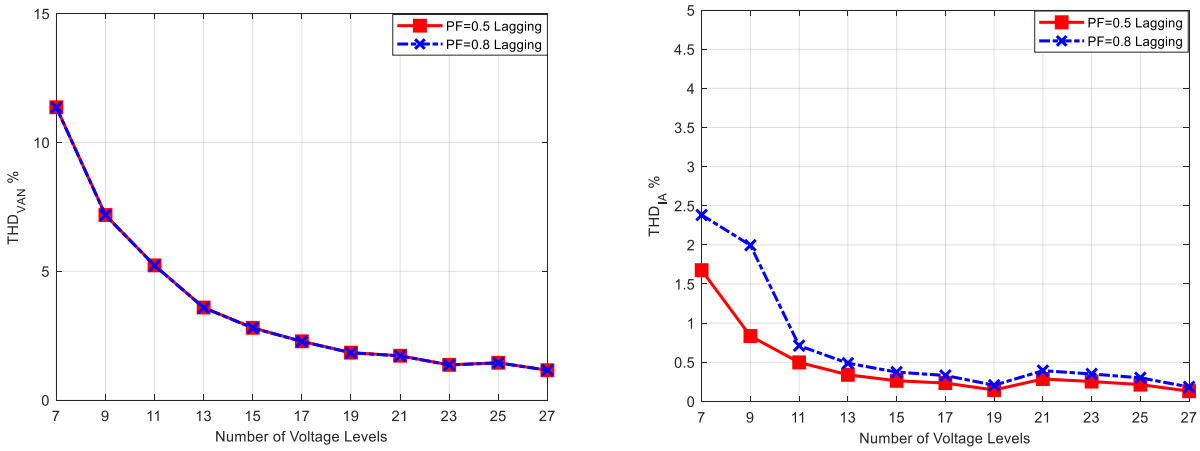


Figure 7. Dynamic response test during different output voltage waveforms at PF = 0.8



(a) (b)

Figure 8. THD of the output (a) voltage and (b) current of the multilevel CHBVSI at different power factors

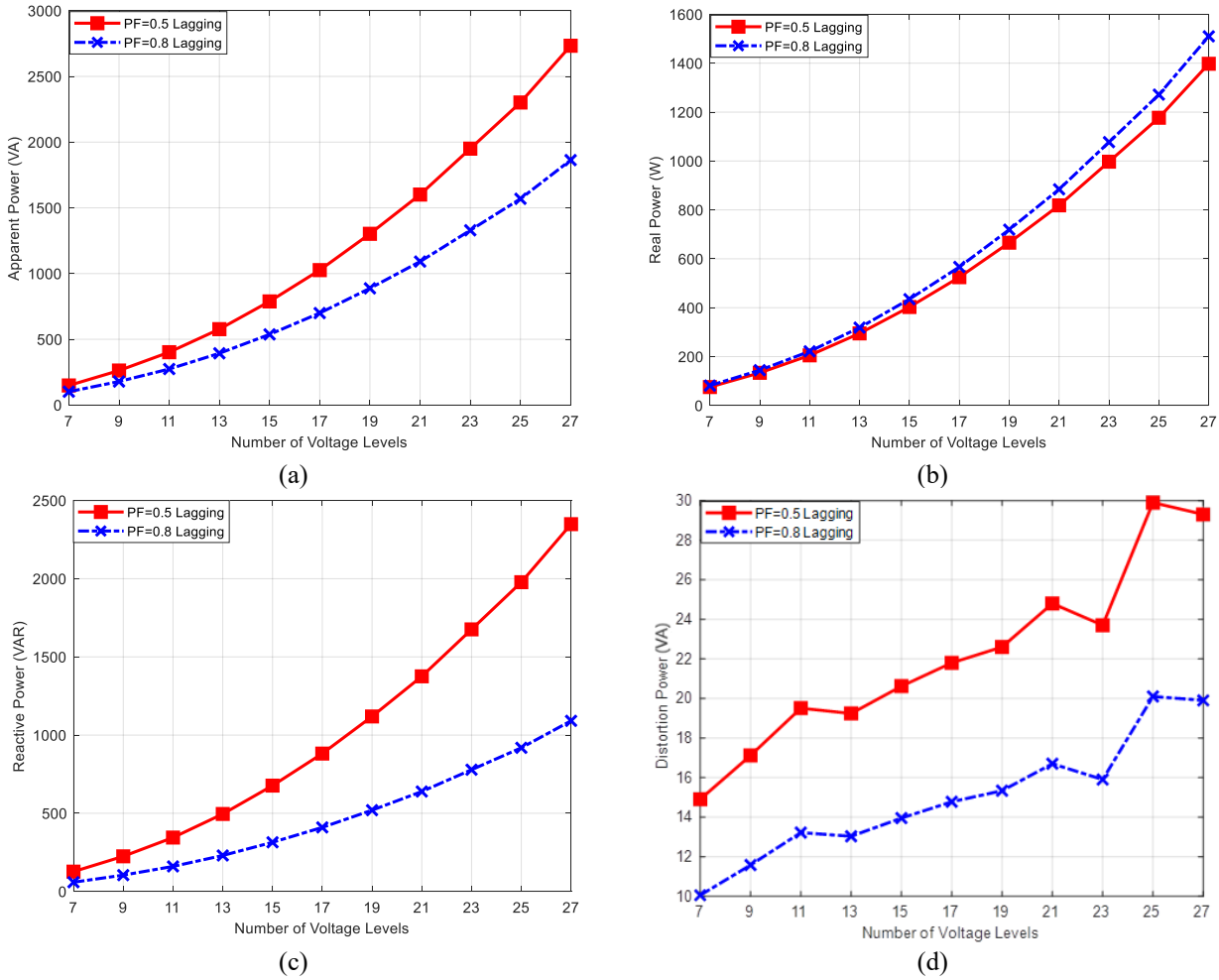


Figure 9. The effect of changing loads at (a) apparent power, (b) real power, (c) reactive power, and (d) distortion power

The overall results illustrated that the THD results using ONE DCVS are within acceptable limits, and the designed circuit is applicable. In the current scope of this work, a simplified magnetic model to isolate and validate the fundamental performance of the proposed MASPWM control strategy and the 27-level topology structure is utilized.

5. CONCLUSIONS

The primary objective of this investigation is to demonstrate a single-phase CHMLVSI in various load applications, utilizing a single DCVS. The designed circuit is built to obtain three unequal DC voltages from the OND DCVS. The circuit has been used with three cells of an H-bridge inverter with unequal and selected DCVSs to get a twenty-seven-level output voltage, with a boosted value of DC link voltage compared with the conventional structure type. THD at different voltage levels and loads is presented. Simulation results show that the components of harmonic orders have been minimized; therefore, an *efficient AC power quality supply has been proposed.* The considered power and control circuits in dynamic and steady-state conditions for various output levels have agreeable quality and a low voltage rating of power electronics.

Finally, while this paper establishes the theoretical and simulation-based proof of concept, future research will focus on the construction of an experimental prototype. This will serve to validate the simulation findings and assess the practical robustness of the proposed control algorithm against grid disturbances and parameter mismatches.

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