IIETA International Information and Engineering Technology Association
Advancing the World of Information and Engineering

Instrumentation Mesure Métrologie
Vol. 24, No. 1, February, 2025, pp. 81-88
Journal homepage: http://iieta.org/journals/i2m

Design and Implementation of a High-Performance 850 MHz Class-E Power Amplifier for 5G NR Applications

Ahmad A. Ismael, Mohammad Tariq Yaseen*

Department of Electrical Engineering, Collage of Engineering, University of Mosul, Mosul 41001, Iraq

*Corresponding Author Email: mtyaseen@uomosul.edu.iq

https://doi.org/10.18280/i2m.240109

Received: 30 November 2024
Revised: 7 February 2025
Accepted: 18 February 2025
Available online: 28 February 2025

Keywords:
power amplifiers, push–pull, NB-IoT, dynamic range, peak to average power ratio (PAPR), power added efficiency

ABSTRACT

This paper present class E power amplifier with high output power and excellent linearity and efficiency to meet the requirements of Narrow Band Internet of Things (NB-IoT) Applications. Push pull class E power amplifier at frequency 850 MHz utilizing CaAs FET technology was used to design the proposed power amplifier. The amplifier's efficiency was greatly increased by employing the class E power amplifier and output power was significantly increased by creating the amplifier with push-pull with collecting power technique. The key contribution of this study is the successful mitigation of the voltage-dependent parasitic capacitor Cgd. The addition of a linearization capacitor to the proposed amplifier topology improves its linearity, gain, dynamic range, and stability. The results of comparison with previous research and the results of circuit simulation using the ADS program confirm this, as the simulation results were: 76% PAE and 20 dB power gain, 33 dBm output power and the dynamic range was 10 dBm.

1. INTRODUCTION

The use of modern communication devices has become widespread, extending into many areas of daily life. With the growing demand for communication and Internet services, there is a need for devices that are affordable, power-efficient, and capable of transmitting large amounts of data with high efficiency to meet users' needs. Modern communication systems, from the fifth generation (5G) and beyond, are continuously evolving to meet these demands. As a result, these systems have become increasingly complex and diverse, utilizing a broad spectrum of frequencies to perform various functions and optimize communication system performance. Consequently, it has been necessary to allocate specific frequency bands for these tasks [1-3].

Frequency bands for 5G New Radio (5G NR), which is the air interface or radio access technology of the 5G mobile networks, are Dedicated Frequency Range 1 (FR1), which includes sub-1 GHz frequency bands, some of which are traditionally used by previous standards, but has been extended to cover potential new spectrum offerings from 410 MHz to 7125 MHz [4, 5]. The 850 MHz frequency band, commonly used for 4G LTE communications, is also essential for 5G and future systems. As part of the low-band spectrum (sub-1 GHz), it offers wide coverage and strong penetration through buildings, making it ideal for rural and indoor 5G deployments where reliability is more important than high data speeds. It ensures backward compatibility with 4G LTE networks, allowing smooth communication during the 5G transition. Additionally, the 850 MHz band is well-suited for IoT and Machine-to-Machine (M2M) communication provide reliable, long-range connection for low-power gadgets such as sensors and smart meters [6-9].

One of the important challenges in designing a communication system for use in IoT applications, especially when these systems operate at a high data transfer rate, is that this makes the information signal have a wide range of variation between a maximum and minimum value measured by PAPR, in addition to a wide bandwidth. This in turn makes the design of the power amplifier a significant task in order to achieve linearity and efficiency suitable for this type of signal.

Therefore, the researchers were involved in developing this part of the system to be at an acceptable level of performance, and to operate with reliability that is compatible with this generation of communications. From the research that dealt with the subject of studying the power amplifier in these applications. The study [6] addresses the difficulty of creating a wideband CMOS power amplifier that functions well and linearly in the 700 MHz to 920 MHz frequency range, which is essential for LTE applications. As a result, this study show that the CMOS power amplifier achieves excellent efficiency and good linearity over the whole frequency range, making it appropriate for LTE applications. The problem of increasing RF power amplifier efficiency by manipulation of second and third harmonics is the subject of another study [7]. Traditional amplifiers often struggle with efficiency, especially across broader bandwidths. This study addresses the issue by implementing a continuous mode design approach, where the amplifier's performance is enhanced by carefully controlling these harmonic components. The results show that this method leads to significantly higher efficiency and good linearity, making the amplifier suitable for modern wireless communication systems, thus demonstrating the effectiveness of harmonic manipulation in achieving high-efficiency RF

amplification. The problem of creating a power amplifier that functions well and linearly over a wide frequency range essential for contemporary cellular base stations is addressed in another work [8]. The study addresses this issue by improving the amplifier's performance over a number of bands utilizing sophisticated design approaches such as wideband impedance matching architecture. The results show that the broadband amplifier is suitable for improving the performance of cellular base stations in contemporary communication systems because it achieves excellent efficiency, linearity, and output power over the intended frequency range.

In this research paper, a power amplifier using GaAS technology is presented. Despite the high cost of GaAS technology and the difficulty of using it in integrated circuits, it is considered suitable for use to obtain high output power and suitable linearity, because this technology has high conductivity and has a high breakdown voltage. This research focuses on the design of a high-power amplifier with enhanced efficiency and linearity. The output power was increased using push-pull amplifier technology, which leverages transformer power combining to achieve power gain. The implementation of Class-E switching power amplifier technology played a crucial role in improving efficiency. Additionally, emphasis was placed on enhancing the amplifier's linearity and stability by mitigating the effects of the parasitic gate-drain capacitance (Cgd) through the use of a cross-coupling capacitor technique. The designed amplifier demonstrated adequate output power, efficiency, and linearity for urban use. The research is structured with an introduction highlighting its significance, followed by the theoretical foundation for designing a class E amplifier in Chapter two, the construction details in Chapters three, results analysis in chapter four and conclusions in Chapter five.

2. BASIC CIRCUIT DESIGN AND WAVE SHAPING

The Class-E power amplifier is considered one of the switched mode power amplifiers that has garnered significant attention from researchers due to its high output power and high efficiency, which can reach up to 100% in ideal conditions [2, 9, 10]. The Basic circuit consists of the load circuit and a transistor represented in the circuit as a switch controlled by the signal applied to the transistor's gate. The load circuit consist of wave shaping and matching circuit. The wave-shaping circuit consists of RF chock (L1) and capacitor (C1) in parallel with the transistor and a series resonant circuit that composed of (LS, CS) allows only the fundamental component to reach the load. The function of the wave-shaping circuit is to reduce the overlap between the voltage and current waveforms inside the transistor to minimize the power losses. The matching network's role is to deliver power from the output of the wave-shaping circuit to the 50-ohm load with minimal losses as shown in Figure 1(a). Considering that the circuit in Figure 1 has ideal components and the transistor works as a switch, the circuit behavior can be explained as follows: During the first half-cycle, when the transistor is in the on state, the transistor's voltage is zero, and current flows through the transistor according to the input voltage, thus forming the current waveform of transistor. The capacitor (C1) completes its charge during the transition period between off and on with a time constant of zero in the ideal case. In the second half-cycle, when the transistor switches to the off state, the capacitor discharges its charge through the series resonant circuit and the RL resistance, resulting in the formation of the voltage waveform across the transistor. Figure 1(b) shows the drain current and voltage waveforms for the class E power amplifier. This scenario represents the process of building the voltage and current wave across the transistor Vs and Is respectively, but in practice This circuit suffers from some practical issues due to the presence of parasitic elements, which cause delays in the transistor's switching and, consequently, affect the signal shape and reduce the amplifier's efficiency. Additionally, the presence of the capacitor (C1) limits its operation at high frequencies [11]. Through this research, a series of ideas are offered in order to tackle these issues and produce a power amplifier with optimal performance.

2.1 Basic circuit design

To construct a class E power amplifier circuit, all components of the amplifier must be integrated perfectly to achieve the desired objective. This requires selecting the appropriate transistor and determining its bias voltages at the operating frequency and the required output power. After that, the bias circuit and load network are designed. In this research, a GaAsFET transistor was used. The optimal transistor bias voltages and output power were obtained using the optimization feature in the ADS simulation software after building the simulation circuit designed for this purpose. The results are shown in Table 1.

Table 1. The optimal transistor bias voltages and output power

PAE (%)	Gate Voltage	Drain Voltage	Power Output
32.78%	-1.75V	3V	0.556 Watts

Based on these values and using the mathematical foundation for calculating the components of both the bias circuit and the load network from Equations 1 to 5. The RF choke (L1) must have a sufficiently high value to prevent AC current from passing to the DC source. The values of Ls, and Cs should be selected to form a resonant circuit that allows the fundamental frequency to pass through with a high-quality factor (Q). In this design, we consider Q=10. Additionally, the value of the parallel capacitor in the wave shaping circuit should be calculated to achieve zero voltage switching (ZVS). The basic amplifier circuit was constructed as shown in Figure 1.

The following equations show the method of calculation [12-15]. The calculation results are shown in Table 2.

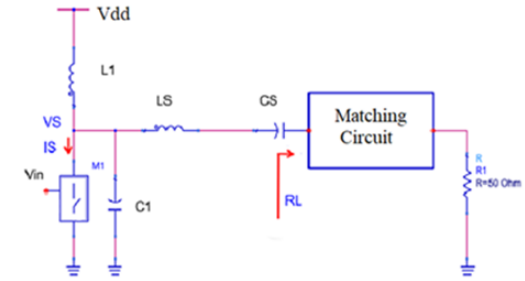
$$R_L = \frac{8(Vdd)^2}{(\pi^2+4)P_o} \quad (1)$$

$$C_1 = \frac{1}{\omega R_L\left(\frac{\pi^2}{4}+1\right)\frac{\pi}{2}} \quad (2)$$

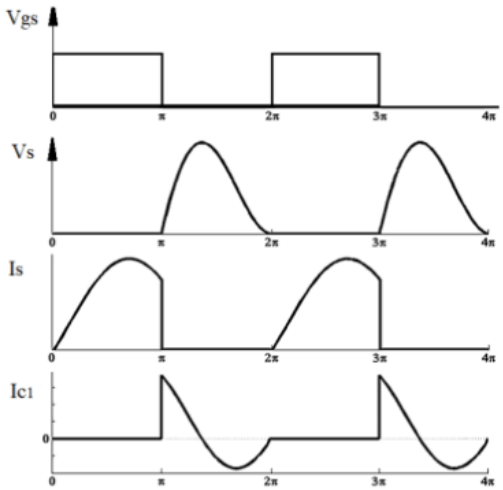
$$L_1 = \frac{100R_L}{\omega} \quad (3)$$

$$C_s = \frac{1}{\omega R_L\left(Q-\frac{\pi(\pi^2-4)}{16}\right)} \quad (4)$$

$$L_s = \frac{QR_L}{\omega} \quad (5)$$



(a) The basic circuit



(b) The voltage and current waveform across the transistor formed with the gate voltage [2]

Figure 1. Basic circuit

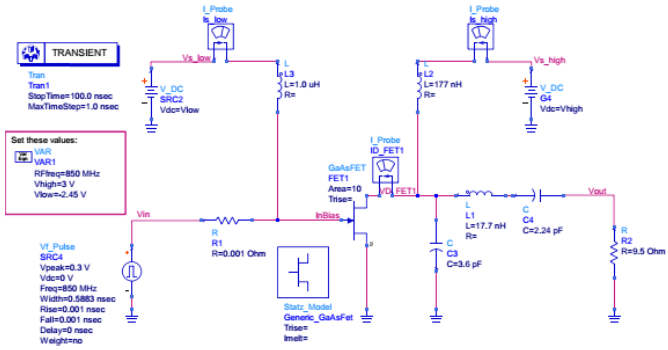
Table 2. Class-E power amplifier results of calculating the components

$R_L\ \Omega$	$C_1\ pF$	$L_1\ nH$	$L_s\ nH$	$C_s\ pF$
9.5	3.6	177	17.7	2.24

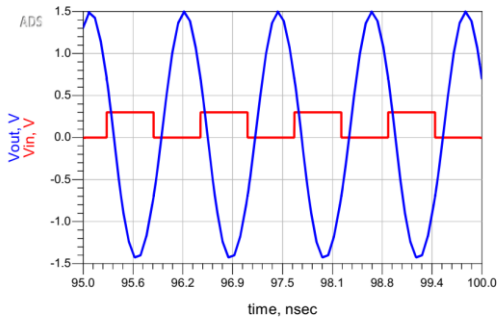
2.2 Wave shaping design

After constructing the amplifier circuit according to the theoretical values, the voltage and current waveforms were not obtained in their ideal form. This was due to the difference between the ideal state of the transistor, which was assumed, and the natural behavior of the transistor according to its physical characteristics. Therefore, some adjustments had to be made to improve the shape of the voltage and current waveforms through the transistor and to reduce the overlap between them, aiming to achieve the lowest possible current through the transistor. The waveform was improved by adjusting the values of gate bias (Vgs), the amplitude (Vp) and duty cycle (D) of pulse function, where the effect of the gate bias point was significant on the maximum transistor current and the maximum voltage observed across the transistor (VDS). Another important point that contributed to the improvement of the voltage and current waveforms was the amplitude and duty cycle of the input signal [12, 16].

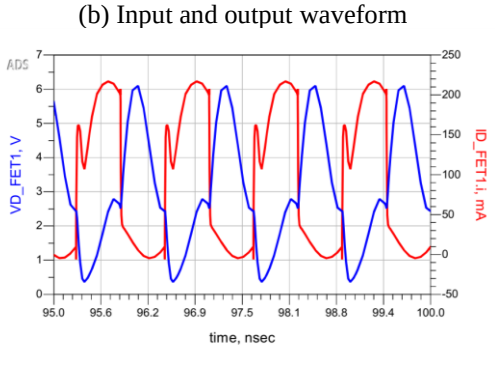
The ideal values of duty cycle (D), amplitude (Vp), and gate bias (VGS) were obtained by using the tune feature after the circuit was constructed using the ADS software. These values were as follows: 0.3 Vp, 50% duty cycle, and VGS = -2.45V, which guarantees the transistor's function as a switch in the circuit and optimally produces the voltage and current waveforms. The circuit and the input and output voltages are displayed in Figure 2.



(a) Basic amplifier circuit



(b) Input and output waveform



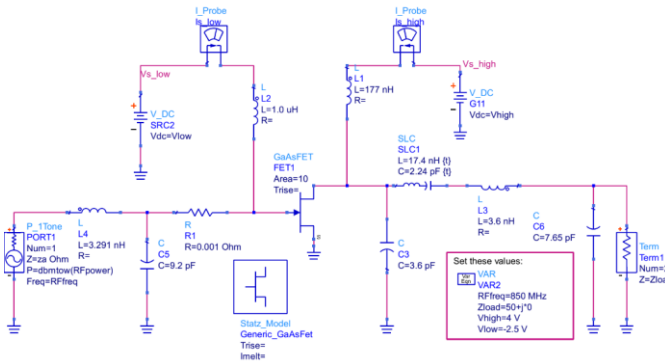
(c) Voltage and current waveform

Figure 2. Basic amplifier circuit with square wave response

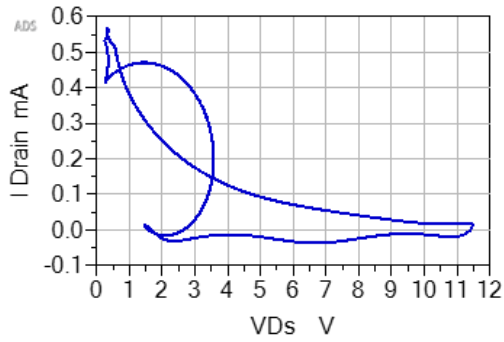
3. IMPLEMENTATION OF A CONTINUOUS CLASS-E MODE

The response of the designed amplifier (PA1) to a square signal as shown in Figure 2(b, c) shows that the amplifier works well through the voltage and current waveform as well as the signal reaching the load. However, the radio signal of modern digital communication systems is a non-constant envelop signal, so it was important to test the amplifier with a real variable-amplitude signal that is compatible with the use of the amplifier in communication systems (long term evaluation LTE). The designed amplifier was tested after matching the input and output to the load and source impedance with a Harmonic Balance Simulation test (HB). However, the amplifier showed poor characteristics because the transistor was losing part of its characteristics as an ideal switch. To address this problem, the ideal value for the gate voltage (Vgs) was chosen to control the connection angle. The ideal value was (-2.5V) so that the connection would be at an angle of ($180 \geq \alpha \geq 360$) where α is the connection angle for the transistor to operate between class (B) and (AB). Farther more

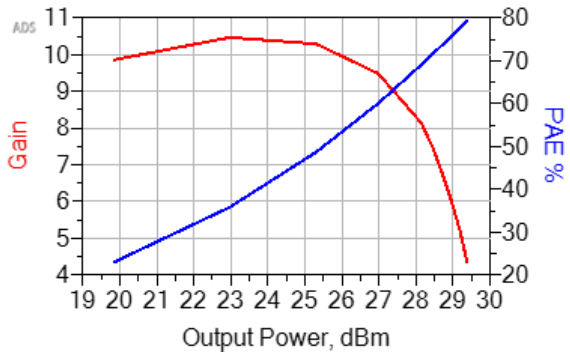
the value of Vdd is tuned to 4V, this contributed significantly to improving the characteristics of the amplifier in terms of linearity and increased output power in addition to providing a flexible open and close pattern for the transistor (Soft Switching Mode) as in Figure 3.



(a) The basic circuit of the power amplifier PA1



(b) The transistor's switching pattern



(c) The gain and power added efficiency (PAE) response with output power

Figure 3. Basic circuit of power amplifier PA1 and its response to a single-tone harmonic balance test

3.1 Power combining implementation

The power combining technique was used to increase the output power in order to expand the scope of use of the designed power amplifier in a wider range of fifth generation applications using (PA2) circuit of Figure 4. A transformer on the input side of the amplifier circuit was used in the design of the amplifier input circuit to distribute the input power evenly between two Class (E) amplifiers. The power was then amplified and combined using an output transformer, which was then connected to the matching circuit to effectively send the power to the load. The circuit showed an unsatisfactory response to the Harmonic Balance Simulation test in terms of gain and efficiency of the added power, especially in the low power region, because the transistor operates for half a cycle and is in the (off) state in the second half, so the Class (E) power amplifier in this circuit will operate with a non-continuous signal, which in turn weakens the amplifier's characteristics. The characteristics of the designed amplifier need to be improved to work in future generations of communication system. Therefore, the alternative solution was to use the push pull technique to improve the power and increase the linearity. By connecting the matching and wave forming circuits to the power combining transformer's output. The push pull amplifier construction is employed in PA3 as shown in Figure 5. The amplifier will therefore be able to handle both the positive and negative portions of the amplified signal. As a result, the signal may be amplified to a greater range, improving linearity, gain, and output power [17].

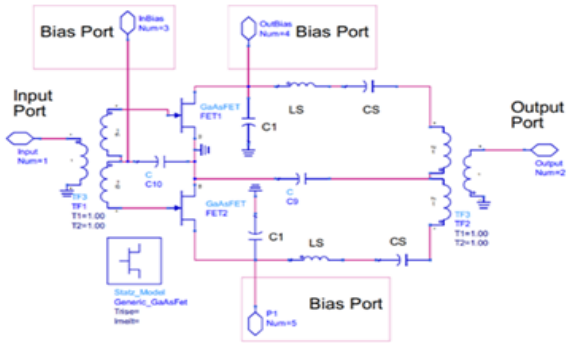


Figure 4. Class E power amplifier with power combining Implementation (PA2)

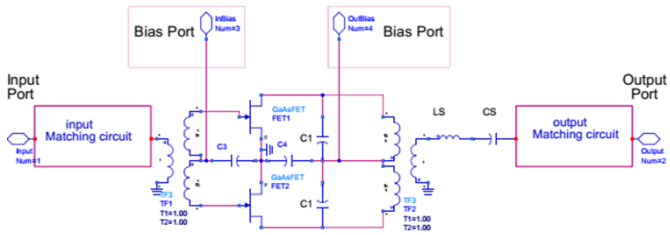


Figure 5. PA3 push pull class E power amplifier

3.2 Capacitor linearization improvement

The characteristics of the power amplifier are greatly affected by the presence of parasitic capacitors because these capacitors make the amplifier start a non-linear response with the change in frequency and amplitude of the information signal. This negatively affects the linear characteristics of the amplifier. The linear characteristics is very important in next generation communication applications due to the need for high linearity and wide bandwidth amplifiers [18-20].

One of the most important capacitors on the characteristics of the amplifier is the capacitor (Cgd), whose value changes depending on the voltage applied to it [21]. This capacitor works to return part of the output voltage to the input side, which in turn reduces the gain and contributes to reducing the isolation between the input and output sides in addition to increasing the effect of the change in the amplitude of the information signal on the linearity of the amplifier as a result of the change in the value of the capacitor with the voltage applied across it. The nonlinear behavior of the gate-drain capacitance (Cgd) in GaAs significantly affects the performance of RF power amplifiers, primarily due to its

voltage dependence. This nonlinearity, intensified by the Miller effect, leads to several performance issues. One major concern is linearity degradation, where the dynamic variations in Cgd distort the output waveform, introducing intermodulation distortion (IMD). Additionally, the voltage-dependent nature of Cgd affects transconductance and input capacitance, causing gain compression and impacting signal amplification. Another issue arises from the unintended feedback created by Cgd, which can shift signal phases unpredictably, potentially leading to oscillations and compromising amplifier stability. To mitigate these nonlinear effects, a cross-coupling capacitor (Cx) is introduced between the gate and drain. This capacitor plays a crucial role in stabilizing the effective capacitance by counteracting variations in Cgd, improving overall linearity.

Despite its advantages, implementing Cx presents certain challenges. Its effectiveness depends on precise tuning to achieve the right balance in linearization without introducing new distortions. Furthermore, while Cx can enhance performance at specific frequencies, it may impose bandwidth limitations if not optimized correctly. The designed circuit structure (PA3) was utilized by connecting a compensating capacitor called Cross-coupling capacitor (Cx) This compound circuit is described as the PA4 amplifier as shown in Figure 6. Due to the configuration of capacitor (Cx) and its interaction with capacitor (Cgd) in the amplifier circuit, it was determined that the combined value of the two capacitors results in a lower equivalent capacitance. This reduction, in turn, leads to increased gain and improvements in the amplifier's linearity and stability. The power amplifier "maximum available gain"[22] could be obtained as:

$$G_{MAX} = \frac{\sqrt{\omega^2(C_{gd}-C_x)^2+g_m^2}}{\omega|C_{gd}-C_x|} \quad (6)$$

"Maximum stability gain" (MSG) and the stability factor (k) are achieved as Eqs. (7) and (8). MSG could be increased when Cx and Cgd are equal:

$$K = \frac{R_g R_d \omega^2 (C_{gd}-C_x)^2+2}{R_g R_d \omega |C_{gd}-C_x| \sqrt{g_m{}^2+(C_{gd}-C_x)^2\omega^2}} \quad (7)$$

$$MSG = \frac{\sqrt{g_m{}^2+(C_{gd}-C_x)^2\omega^2}}{|C_x-C_{gd}|\omega} \quad (8)$$

After testing the circuit, it was found that adding the capacitor has a direct effect in improving the amplifier's characteristics in terms of gain and linearity. The harmonic balance test was used to compare the performance of the power amplifiers (PA3) and (PA4). The results of the comparison demonstrated that the power amplifier (PA4) improved the dynamic range of the amplification, increased the gain, and increased the output power, confirming the efficacy of using the cross-coupling capacitor more effectively.

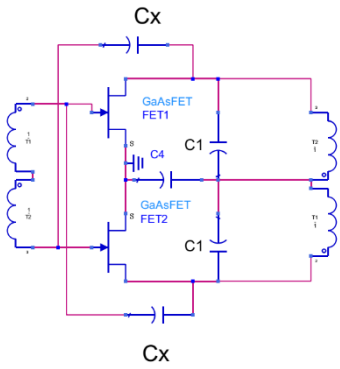


Figure 6. Push pull class E power amplifier with cross-coupling capacitor **(**PA4)

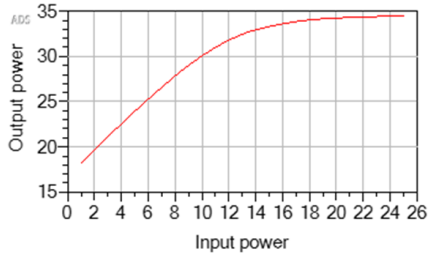
4. RESULTS

According to the requirements of modern communication systems, linearity, output power and efficiency are considered the most important factors that are focused on in the design of the power amplifier.

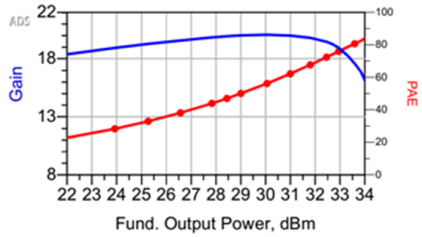
Therefore, these specifications were focused on to improve the performance of the power amplifier until the proposed power amplifier was reached in its final form. The amplifier (PA1) was an (E) type amplifier with somewhat acceptable efficiency and linearity, but the output power was insufficient, so the amplifier (PA2) was developed to work on increasing the power by applying the power combining technique, but this amplifier did not achieve the designed goal because the amplifier output circuit and the matching circuit were dealing with the output of each transistor separately, and thus the amplifier appeared as if it were a half-wave amplifier, which in turn reduces the efficiency and output power, and this is clear from the results of (PA2) in Table 3. This problem was addressed by using the power amplifier (push pull) with the power amplifier type (E) to collect the power and send it to the load through the matching circuit that deals with the amplifier output signal with its positive and negative parts, which greatly improves the response, and the results of the power amplifier (PA3) were in Table 3. The power amplifier (PA3) was developed by reducing the effect of the capacitor (Cgd) in order to expand the possibility of using the proposed amplifier in many applications. The capacitor (Cx) was added as in (PA4), where this technique contributed to improving the gain, efficiency, output power and increasing the amplifier's dynamic range. The results of the power amplifier (PA4) to the single tone harmonic balance test are shown in Figure 7. Figure 7 illustrates the variation in output power relative to input power, showing that the amplifier achieves a maximum gain of 20 dB at an output power of 29 dBm. The dynamic range of the amplifier is 10 dBm, spanning from a maximum output power of 33 dBm to 23 dBm, with a gain deviation of less than 1 dB from the peak gain.

Table 3. Comparison of single tone harmonic balance test results for proposed amplifiers

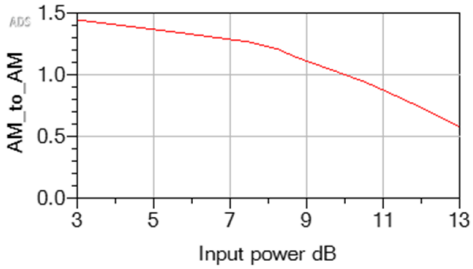
	Gain dB	VDD V	PAE @p_{max}	PAE @p_{min}	Pout Max	DR dBm	THD dBc	AM/AM dB/dB	AM/PM degrees/dB	FOM %
PA1	10	4	60	24	27	7	-50	0.5 - 0.9	(-0.6)- (-0.3)	67
PA 2	6	4.8	30	12	23	8	-47	0.5 – 1.3	(-1.1)- (0.5)	43.7
PA 3	19	4.8	71	32	31	8	-39	0.7 – 1.4	(-0.5)- (0.5)	67.1
PA 4	20	4.8	76	28	33	10	-33	0.6 – 1.4	(0.1)- (0.3)	81



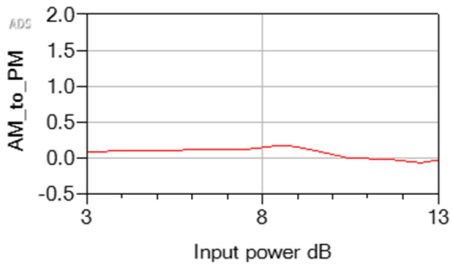
(a) Variation output power with respect to input power



(b) Variation in Gain, PAE with respect to output power



(c) Variation in AM/AM distortion as a function of input power



(d) Variation in AM/PM distortion as a function of input power

Figure 7. PA4's response to single tone harmonic balance test

Table 4. A comparison of the proposed amplifier's results with those of other studies employing various techniques for NB-IoT applications

Reference	Supply (V)	Pout Max dBm	PAE % @P_{Max}	Gain dB	Techniques
[2]	3.3	31.1	58.1	23	Push pull Class-E/F
[3]	1	16.5	51.3	21.6	Class D
[17]	4	27	47.4	13.3	Doherty
[22]	1.8	29.5	43.5	36	Class-E
[23]	3.3	27.7	44.3	24.1	Load Modulation
[24]	3.3	28.8	57.8	20.4	Parallel-combined transistor
[25]	3.3	27	44.4	29.3	Bias Modulation
[This work]	4	33	76	20	Push pull class E

In terms of linearity, the (AM/AM) distortion for amplifier (PA4) has improved compared to the initial design, as highlighted in Table 3. As for (AM/PM) variation, the difference is more pronounced. Despite the amplifier's wide dynamic range, the (AM/PM) variation remains within the range of (0.1) to (0.3), clearly indicating enhanced linearity for amplifier (PA4). Due to the nature of the power added efficiency (PAE) response, where the PAE decreases with the reduction of the output power, increasing the amplifier's dynamic range had an adverse effect on the power added efficiency, where we find that it decreased from (32%) in the case of (PA3) to (28%) in the final proposed power amplifier (PA4).

Power-Added Efficiency (PAE) is a fundamental performance metric in RF power amplifier design, measuring the efficiency with which DC power is converted into useful RF output power. Several factors influence observed PAE values, including transistor efficiency, harmonic management, biasing conditions, load matching, and thermal effects. The choice of GaAsFET transistors plays a crucial role due to their low on-resistance and high breakdown voltage, which help minimize power dissipation. The class E configuration, benefiting from switch-mode operation, minimizes conduction losses and improves drain efficiency. However, any mismatch between the amplifier and the output load results in reflected power losses, significantly reducing PAE. Additionally, excessive heat dissipation can lead to gain compression and efficiency degradation, further limiting overall performance.

Due to the nature of the power added efficiency (PAE) response, where the PAE decreases with the reduction of the output power, increasing the amplifier's dynamic range had an adverse effect on the power added efficiency, where we find that it decreased from (32%) in the case of (PA3) to (28%) in the final proposed power amplifier (PA4).

Many research has addressed the design of power amplifiers for usage in low-band frequencies for a variety of applications, including machine-to-machine and network communication as well as Internet of Things connectivity [26-28]. The amplifier was constructed by the researchers using a variety of methods. As shown in Table 4, the results of the planned research were compared with the results of previous studies. The results showed that the amplifier was developed with characteristics that make it suitable for use in a wide range of applications.

5. CONCLUSIONS

Numerous studies have concentrated on designing power amplifiers for low-band frequency applications, including machine-to-machine, network, and Internet of Things communications, and this is due to the importance and novelty of the subject. This study focused on building a high-performance power amplifier in terms of efficiency, linearity and output power. The selection of GaAs technology with the

use of push-pull with transformer power combiner technology played an important role in producing high power. The class E power amplifier technology also contributed to significantly improving the efficiency of the amplifier due to the property of this type of amplifier in reducing the interference between the voltage and current wave to reduce power losses due to the switched mode of the amplifier. The linearity of the amplifier was significantly improved as a result of reducing the effect of the Cgd capacitor value by adding the cross-coupling capacitor (Cx), which contributed to reducing the effect of the Cgd capacitor value by the input signal, and lead to reducing the sensitivity of the amplifier to changes in the amplitude and frequency of the input power. This in turn pushed the amplifier to operate in a wider range of power, which expanded the dynamic range of the amplifier in addition to increasing the band width of the proposed power amplifier. The results were suitable for using the designed amplifier in modern communication systems, as shown by the comparison results with previous works.

ACKNOWLEDGEMENT

The authors express their sincere gratitude to the Department of Electrical Engineering, College of Engineering, University of Mosul, for their invaluable support in the completion of this work.

REFERENCES

[1] Skokowski, P., Malon, K., Kryk, M., Maślanka, K., Kelner, J.M., Rajchowski, P., Magiera, J. (2024). Practical trial for low-energy effective jamming on private networks with 5G-NR and NB-IoT radio interfaces. IEEE Access, 12: 51523-51535. https://doi.org/10.1109/ACCESS.2024.3385630

[2] Medhat, M., Hussien, F., El-Ghoneimy, M.R., Mohieldin, A.N. (2022). A fully-integrated 40 nm CMOS 58.1% PAE push-pull Class-E/F odd power amplifier for NB-IoT applications. In 2022 29th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Glasgow, United Kingdom, pp. 1-4. https://doi.org/10.1109/ICECS202256217.2022.9971087

[3] Harifi-Mood, M., Bijari, A., Alizadeh, H., Forouzanfar, M., Kandalaft, N. (2021). Power efficiency enhancement analysis of an inverse class D power amplifier for NB-IoT applications. Analog Integrated Circuits and Signal Processing, 107: 551-565. https://doi.org/10.1007/s10470-021-01807-0

[4] Qi, T., He, S. (2019). Power up potential power amplifier technologies for 5G applications. IEEE Microwave Magazine, 20(6): 89-101. https://doi.org/10.1109/MMM.2019.2904409

[5] Yaseen, M.T. (2021). Light harvesting enhancement using metal nanoparticles. Eastern-European Journal of Enterprise Technologies, 2(5): 110.

[6] Chiou, H.K., Lin, H.C., Chang, D.C. (2023). High-efficiency and cost-effective 10 W broadband continuous class-J mode Quasi-MMIC power amplifier design utilizing 0.25 μm GaN/SiC and GaAs IPD technology for 5G NR n77 and n78 bands. Electronics, 12(16): 3494. https://doi.org/10.3390/electronics12163494

[7] Jiang, Z., Chen, D., Zhou, Y., Liu, Z., Zhao, C., Kang, K. (2018). A 700 MHz-920 MHz CMOS power amplifier for LTE applications. In 2018 International Conference on Microwave and Millimeter Wave Technology (ICMMT), Chengdu, China, pp. 1-3. https://doi.org/10.1109/ICMMT.2018.8563705

[8] Ali, F.M., Al-Muifraje, M.H., Saeed, T.R. (2021). High efficiency continuous mode RF power amplifier based on second and third harmonic manipulation. International Journal of Microwave and Wireless Technologies, 13(3): 223-233. https://doi.org/10.1017/S1759078720001002

[9] Ahmed, S.A., Ikechiamaka, F., Akinsanmi, A. (2020). Broadband power amplifier for cellular base station application. International Journal of Engineering Science and Application, 7(3): 64-71. https://doi.org/10.1109/ANDESCON50619.2020.9272187

[10] Casallas, I., Páez, C., Fajardo, A., Perilla, G. (2020). Design methodology of Class-E power amplifier using feed inductance tuning for high-efficiency operation in wireless power transfer applications. In 2020 IEEE ANDESCON, Quito, Ecuador, pp. 1-6. https://doi.org/10.1109/ANDESCON50619.2020.9272187

[11] Barzgari, M., Ghafari, A., Nikpaik, A., Medi, A. (2021). Even-harmonic class-E CMOS oscillator. IEEE Journal of Solid-State Circuits, 57(6): 1594-1609. https://doi.org/10.1109/JSSC.2021.3124971

[12] Sadeque, M.G., Yusoff, Z., Roslee, M., Hadi, N.S.R. (2019). Design of a broadband continuous class-F RF power amplifier for 5G communication system. In 2019 IEEE Regional Symposium on Micro and Nanoelectronics (RSM), Pahang, Malaysia, pp. 145-148. https://doi.org/10.1109/RSM46715.2019.8943508

[13] Yusop, Y., Saat, M.S.M., Husin, S.H., Nguang, S.K., Hindustan, I. (2016). Design and analysis of 1MHz class-E power amplifier for load and duty cycle variations. International Journal of Power Electronics and Drive Systems, 7(2): 358. http://dx.doi.org/10.11591/ijpeds.v7.i2.pp358-368

[14] Karabulut, A., Dogan, O., Ozdemir, S. (2020). Designing and analysis of an optimal capacitive power system using class-E power amplifier. SSRG International Journal of Mechanical Engineering. https://doi.org/10.14445/23488360/IJME-V7I3P102

[15] Afanasyev, P., Grebennikov, A., Farrell, R., Dooley, J. (2020). Analysis and design of outphasing transmitter using class-E power amplifiers with shunt capacitances and shunt filters. IEEE Access, 8: 208879-208891. https://doi.org/10.1109/ACCESS.2020.3038584

[16] Abdullah, F.Y., Yaseen, M.T., Huseen, Y.M. (2021). Portable heartbeat rate monitoring system by WSN using LabVIEW. International Journal of Computing and Digital Systems, 10: 353-360.

[17] Casallas, I., Paez-Rueda, C.I., Perilla, G., Pérez, M., Fajardo, A. (2021). Design of the class-E power amplifier with finite DC feed inductance under maximum-rating constraints. Applied Sciences, 11(9): 3727. https://doi.org/10.3390/app11093727

[18] Hayati, M., Roshani, S., Roshani, S., Kazimierczuk, M.K., Sekiya, H. (2017). Design of class E power amplifier with new structure and flat top switch voltage waveform. IEEE Transactions on Power Electronics, 33(3): 2571-2579.

http://doi.org/10.1109/TPEL.2017.2698834
[19] Cho, Y., Moon, K., Park, B., Kim, J., Kim, B. (2016). Voltage-combined CMOS Doherty power amplifier based on transformer. IEEE Transactions on Microwave Theory and Techniques, 64(11): 3612-3622. https://doi.org/10.1109/TPEL.2017.2698834
[20] Gu, L., Zulauf, G., Zhang, Z., Chakraborty, S., Rivas-Davila, J. (2020). Push–pull class Φ2 RF power amplifier. IEEE Transactions on Power Electronics, 35(10), 10515-10531. https://doi.org/10.1109/TPEL.2020.2981312
[21] Sotiriadis, P.P., Adamopoulos, C.G., Baxevanakis, D., Zarkos, P.G., Vassiliou, I. (2020). RF switched-capacitor power amplifier modeling. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 40(8): 1525-1530. https://doi.org/10.1109/TCAD.2020.3025207
[22] Abbasi, H., Hayati, M., Kazimierczuk, M.K., Sekiya, H. (2020). Design of class-EM amplifier with consideration of parasitic non-linear capacitances and on-state resistance. IET Power Electronics, 13(14): 3065-3071. https://doi.org/10.1049/iet-pel.2020.0253
[23] Kang, H., Udrea, F. (2020). Dynamic CGD and dV/dt in Superjunction MOSFETs. IEEE Transactions on Electron Devices, 67(4): 1523-1529. https://doi.org/10.1109/TED.2020.2974853
[24] Ghorbani, A.R., Ghaznavi-Ghoushchi, M.B. (2018). A low-area, 43.5% PAE, 0.9 W, Class-E differential power amplifier in 2.4 GHz for IoT applications. Integration, 61: 178-185. https://doi.org/10.1016/j.vlsi.2017.12.006
[25] Ahn, H., Oh, K., Choi, S.E., Son, D.H., Nam, I., Lim, K., Lee, O. (2024). A dual-mode CMOS power amplifier with an external power amplifier driver using 40 nm CMOS for narrowband internet-of-things applications. Nanomaterials, 14(3): 262. https://doi.org/10.3390/nano14030262
[26] Lim, W., Kang, H., Lee, W., Bae, J., Oh, S., Oh, H., Chae, S., Hwang, K.C., Lee, K.Y., Yang, Y. (2018). Dual-mode CMOS power amplifier based on load-impedance modulation. IEEE Microwave and Wireless Components Letters, 28(11): 1041-1043. https://doi.org/10.1109/LMWC.2018.2871339
[27] Hussein, S.H., Yaseen, M.T. (2021). Performance evaluation of low-voltage CMOS switched-capacitor circuit. In 2021 8th International Conference on Electrical and Electronics Engineering (ICEEE), Antalya, Turkey, pp. 40-43. https://doi.org/10.1109/ICEEE52452.2021.9415921
[28] Rawat, A.S., Rajendran, J., Mariappan, S., Shasidharan, P., Kumar, N., Yarman, B.S. (2022). A 919 MHz—923 MHz, 21 dBm CMOS power amplifier with bias modulation linearization technique achieving PAE of 29% for LoRa application. IEEE Access, 10: 79365-79378. https://doi.org/10.1109/ACCESS.2022.3193689

NOMENCLATURE

R_L	Load resistance
Q	quality factor
G_{MAX}	maximum available gain
MSG	Maximum stability gain
Cx	called Cross-coupling capacitor

Greek symbols

α	connection angle
Ω	ohm
ω	radian frequency