IIETA International Information and Engineering Technology Association
Advancing the World of Information and Engineering

Journal Européen des Systèmes Automatisés
Vol. 57, No. 2, April, 2024, pp. 599-608
Journal homepage: http://iieta.org/journals/jesa

Realization of IIR Digital Filter Structures for ECG Denoising

Noor Talal Gadawe, Rasha Waleed Hamad, Sahar Lazim Qaddoori*

Electronic Engineering Department, Electronics Engineering College, Ninevah University, Mosul 41001, Iraq

Corresponding Author Email: sahar.qaddoori@uoninevah.edu.iq

https://doi.org/10.18280/jesa.570228

Received: 14 March 2024
Revised: 1 April 2024
Accepted: 12 April 2024
Available online: 28 April 2024

Keywords:
FPGA, IIR filter structures, lattice ladder, retiming, xilinx system generator

ABSTRACT

This research is concerned with applying a reconfigurable system for the hardware realization of digital filters. In particular, it rightly questions whether Field-Programmable Gate Arrays (FPGAs) can be effectively used to implement digital Impulse Infinte Response (IIR) filters. Taking direct, cascaded, and parallel structures of IIR filters with standard and retiming techniques as examples to explore some classifications. The application being investigated most closely is electrocardiogram (ECG) signal processing within an FPGA platform. Using the Simulink environment, a digital IIR band-pass filter is designed and simulated within the MATLAB environment. The filter shows commendable performance in heart signal detection within ECG signals. These IIR filter structures can be hardware-implemented by using the Xilinx System Generator (XSG) tool. The target device here is a member of the Artix 7 family, the XC7A100t-1CSG324 FPGA device. Comprehensive hardware utilization metrics, including the number of slices, look-up tables, peak memory usage, and maximum operating frequency, are extracted from the compilation report during this process. The study uses standard and retiming techniques to optimize the efficiency of FPGA-based IIR filter implementations. Thus it provides insight into whether such filters are suitable for real-time ECG signal processing applications.

1. INTRODUCTION

Two important features of digital signal processing systems are real-time requirements and Data-driven execution [1]. The main working process in the area of signal processing is filtering. From this angle, many electronic devices have wide applicability in the use of filtering techniques to remove unwanted frequency components; reduce noise and interference signals; and pick out desired portions from among all others which are included as well within detected waves. Compared with their analog filter counterparts, digital filters also enjoy a number of advantages: small sizes, high efficiency levels and rapid reconfiguration capabilities. Furthermore, they are operationally more precise than analogues under highly accurate operational conditions [2, 3]. As the name implies, a non-recursive filter does not rely on feedback in its operation. This produces a finite impulse response, making it almost equivalent to what an FIR filter would be called. On the other hand, a recursive filter makes use of feedback and has an infinite impulse response. It is thus known as an Infinite Impulse Response (IIR) filter [4, 5]. Compared to a Finite Impulse Response (FIR) filter and IIR filter is generally more efficient at achieving given performance criteria for a particular order of filters. The reason it is so efficient that the IIR filter can take feedback into account and represents both poles and zeros of a system's transfer function, in contrast to which FIR is only an all-zero type [6-10].

Moreover, accelerating the deployment of digital IIR filter structures in real-time signal processing means that Critical Path Delay (CPD) must be minimized or optimized, so long as only delay elements alone may be repositioned. Among the delay elements introduced into this circuit, retiming is distinguished as a transformative algorithm to rearrange these delay elements without changing their input-output characteristics. Thus, retiming has a variety of applications-such as shortening the period or clock cycle in a circuit and reducing registers [11].

Reconfigurable Field Programmable Gate Array (FPGA) technology has grown tremendously from a dedicated hardware to a heterogeneous system which is considered as a popular choice in communication base stations instead of being just a prototype platform [12]. With an IIR filter deployed on a FPGA, there are significant advantages: speed, ease of use, flexible adjustment and quick calculation accuracy. One innovative approach is to integrate a digital IIR structural design into an FPGA, so that high-performance systems can be implemented at low cost [13-15].

The development of digital signal processing methods has markedly changed different fields in particular, in biomedical engineering where it is of utmost significance to precisely process physiological data like ECG (electrocardiogram) signals since these are needed for diagnosis and monitoring. Therefore, digital filters, as a key in achieving the right signal quality and dependability of ECG signal processing system, are called.

So that this study gives the computer field supported approaches to the digital filter, the exploration of FPGA with infinite impulse response digital filter (IIRDIF) platform

viability is the focus. In addition, it considers the one-pole-pole-dharma Infinite Impulse Response signal delay estimators of the Field Programmable Gate Array architectures. Our research aims to evaluate the performance and efficiency of two distinct IIR filter structures: straight, branch, and parallel structures that are operated as is and retimed.

Specifically, this manuscript aims to address the following research questions:

(1) What is the comparative performance of FPGA-based implementations of IIR digital filters, particularly in terms of resource utilization and operating frequency?
(2) What kinds of IIR filter structures like direct, cascaded, parallel, and lattice ladder structures contribute to efficiency and well-working, fast ECG signal processing?

By leveraging the Simulink interface and MATLAB framework, the digital IIR cutoff filters are designed and simulated to analyze heart signal detection within ECG signals. Subsequently, the feasibility of hardware implementation is explored using the Xilinx System Generator (XSG), targeting the Artix 7 family FPGA chip (XC7A100t-1CSG324). Through comprehensive compilation reports, the manuscript aims to extract metrics such as the number of slices, look-up tables, peak memory usage, and maximum operating frequency to evaluate the performance of FPGA-based IIR filters.

Some possible hypotheses that can be investigated in this paper are:

(1) Due to the fact that IIR digital filter structures perform the function of noise removal and the disease scenario recognition, the diagnostic accuracy of the disease will be enhanced.
(2) Nevertheless, the lower-order IIR filters via combining them with higher-order ones can represent a similar effectiveness in echo-canceling which ultimately leads to a reduction in computational complexity.
(3) The current study deals with finding the critical path delay in IIR digital filter structures for impulse and response which is similar to a realization of ECG denoising system.
(4) The investigation of the FPGAs efficient use of hardware resources for suggested different digital filter structures IIR such as direct form, cascade form, and lattice structure while in the platform will demonstrate the high level of efficiency in resource utilization.
(5) Determination of denoising ability in the proposed IIR filter structures is found to be better over the conventional methods by combination of noise removal and maintaining the ECG waveform qualities.

This research is structured as follows: In Section 2, a concise review of relevant previous research is presented. Section 3 provides a complete explanation of the structures for IIR filters and the details of ECG application. Section 4 attaches great importance to the assessment of hardware implementation and offers a comparative analysis of the proposed structures with other methods. Finally, Section 5 presents the most significant conclusions of this study.

2. RELATED WORKS

The critical evaluation of prior research on the art of infinitely moving response (IIR) filters for the ECG signals processing in FGPA architectures is the main aim of this section. This brings us to the subject of clarity communication, and therefore this section has subdivided into subsections because of the different themes highlighted in the literature.

2.1 FPGA implementation of digital filter structures and challenges

This section is dedicated to outlining the process of structure integration of digital filters based on FPGAs. It is about the approaches, design factors, and enchancements used to realize FPGA-based designer achievable and of the highest efficiency and speed.

One method of retiming suitable for fixed-point circuits was proposed by Meher [16]. His idea was to introduce novel node-merging and node-splitting techniques into practical retiming methods, with the objective of shortening the critical path length in the initial data-flow graph. But, this optimization required only a moderate increase in the number of registers (especially for FIR and IIR filter implementations).

The Xilinx System Generator was used in Bujjibabu and Sravani [17] of high-performance recursive filter architectures for low power applications. They focused on implementing a 5th-order low-pass IIR filter in different forms: Cascade form, Direct form-I and Direct form-II. Their comparative analysis looked at power consumption, area, and speed. Reaching the assessment that cascade (Direct form-I) is most appropriate for higher order power constrained filters, and cascade (Direct Form-II), best in area and speed. Pathak et al. [18] have introduced an FPGA implementation of Notch/anti-notch IIR filters with floating point arithmetic. Their design was first synthesized onto a board for the Zynq series FPGA family using Xilinx ISE 14.4, then the simulations were performed with the help of Isim simulator. The test yields give them a 1.56-fold increase in IIR filter performance due to the use of re-timing techniques. Their proposed design exhibited a similar level of precision to that achieved in the MATLAB implementation with the same IIR filter. Seshadri and Ramakrishnan [19] measured various filter configurations including traditional IIR filters with cutoff frequency or order synthesis; high-speed multiplier less IIR implementation at phase one and phase two using look ahead arithmetic; typical Moving Average (MA) FIR filters and fast MA FIR implemented utilizing look ahead weight calculation. These filters were implemented for the Altera EP4CE115F29C7 FPGA platform using Quartus II 13. The simulation results unequivocally show that high-speed IIR and MA FIR filters employing look - ahead arithmetic perform better than their traditional counterparts.

Datta and Dutta [20] detailed their efforts on designing and implementing IIR filters within an FPGA platform. They thus proposed an IIR design utilizing parallel-pipeline architecture and heavily based on FIR filter structure. Moreover, the paper also investigated two modern methods: look-ahead and two-level pipeline IIR filter schemes. These designs were thoroughly detailed in Hardware Description Language (HDL) and extensively verified on the Xilinx Virtex-5 FPGA platform. Their experiment results indicated that in terms of important performance evaluation parameters such as hardware efficiency, operational speed and power consumption the suggested FIR-based IIR configuration outperformed traditional configurations.

2.2 Application of IIR filters in biomedical signal processing

Here, the manuscript delves into prior studies that have explored the application of infinite impulse response (IIR)

filters in biomedical signal processing, with a specific emphasis on ECG signal denoising and analysis. The rationale is examined behind choosing IIR filters for ECG signal processing tasks and highlight the advantages and limitations of existing approaches.

To suppress noise in ECG signals, Gaikwad and Chavan [21] designed indicative of low-pass IIR elliptic digital filter (with a cutoff frequency at 100 Hz). On the FPGA platform, Vedic multiplier is used to implement the filter with XSG. These results reveal advantages in area, power consumption and speed. Mukherjee and Bakshi [22] introduced a method for denoising ECG signal using different filters: the Savitzky-Golay Filter, High Pass Filter and Weighted Window filter combined together. The study underscored the importance of a pre-processing filtering device that denoises ECG signals for accurate diagnosis of heart disease. On the basis of a comparison of filter performances, they concluded that the Savitzky-Golay Filter is suitable for denoising. Ladekar et sl. [23] recommended the use of FPGA technology to implement a more sophisticated form IIR filter for EEG preprocessing. This study focuses on applying retiming and pipelining techniques to these filter structures. Simulate the newly optimized configurations with MATLAB's Simulink and then deploy them on a Virtex-5 FPGA. An analysis of several different structures showed that allpass-based IIR architectures have the lowest computational complexity and CPD, relative to conventional configurations. In addition, these configurations have a lower slice delay product and can handle higher extreme sampling frequencies. However they do need more LUTs (slice lookup tables).

Different structures of IIR filters were presented and implemented using FPGA in this paper. The IIR structures are simulated by XSG tools and hardware resources estimation is performed with the help of ISE14.7 from Xilinx and FPGA artix7 platform.

3. RESEARCH METHOD

In this section, various IIR filter structures with standard and retimed techniques will be explained based on the CPD for IIR filter configuration. Furthermore, how to implement these IIR structures for ECG denoising will be declared.

3.1 IIR filters structures (standard & retimed)

A digital filter is a mathematical method executed using both hardware and software, designed to process a digital input signal and generate a digital output signal with the aim of achieving specific filtering objectives [8, 24]. The IIR filter comprises dual components: a forward FIR filter, commonly known as an 'all-zero filter,' where the numerator coefficients (b) pertain to the zeros, and a feedback FIR filter dealing with the denominator coefficients (a) associated with the poles. An alternative depiction of an IIR filter is through a z-transfer function, which can be expressed as in Eq. (1):

$$H[z] = \frac{Y[z]}{X[z]} = \frac{\sum_{m=0}^{N} b_m z^{-m}}{1 + \sum_{m=1}^{N} a_m z^{-m}} \quad (1)$$

The transfer function necessitates 2N adders and 2N+1 multipliers [25, 26]. The CPD differ across various structures, such as cascade form, direct form, lattice realization, and parallel form, and these delays tend to increase as the filter order rises. Efficient retiming technique reduces the CPD by transforming the original structures. For direct form, shared delays at odd locations are cut and transferred to other edges. Cascade form involves cutsets at each stage and pipelining delay elements. Parallel form requires cutsets in the feedforward path and pipelining before the output adder. Lattice ladder involves pipelining in the output edge and node retiming. The CPD in hardware implementation for Nth order IIR filters is provided in Table 1 for standard and retimed realizations.

Table 1. The CPD for IIR filter configurations

CPD	Original	Retimed
Lattice Ladde	3Tm+(N+3)Ta	Tm+2Ta
Parallel	2Tm+(p2+1)Ta	Tm+2Ta
Cascade	Tm+(2p1+1)Ta	Tm+2Ta
Direct	2Tm+(N+1)Ta	Tm+2Ta

3.2 IIR filter based ECG denoising

In this section, IIR filter structures are implemented for the purpose of ECG denoising and enhancement. The specific IIR filter employed is a bandpass filter with a frequency range of 0.25 Hz to 40 Hz. The bandpass ripple is set at 0.5 dB, and a fourth-order Chebyshev filter type is utilized due to its balance between noise suppression and preserving ECG components. It achieves a sharp roll-off in the stopband while minimizing passband ripple. Higher-order filters introduce more ripple, distorting the ECG. The 4th order filter carefully considers the tradeoff between noise reduction and waveform fidelity. It provides effective denoising while keeping computational requirements reasonable, making it advantageous for real-time processing. Also The sampling rate for this system is 600 Hz. The selection of filter coefficients is based on those provided in the study [8]. The transfer function for the bandpass filter is defined as in Eq. (2):

$$H[z] = \frac{0.0464 - 0.0927z^{-2} + 0.0464z^{-4}}{1 - 3.3523z^{-1} + 4.2557z^{-2} - 2.454z^{-3} + 0.5506z^{-4}} \quad (2)$$

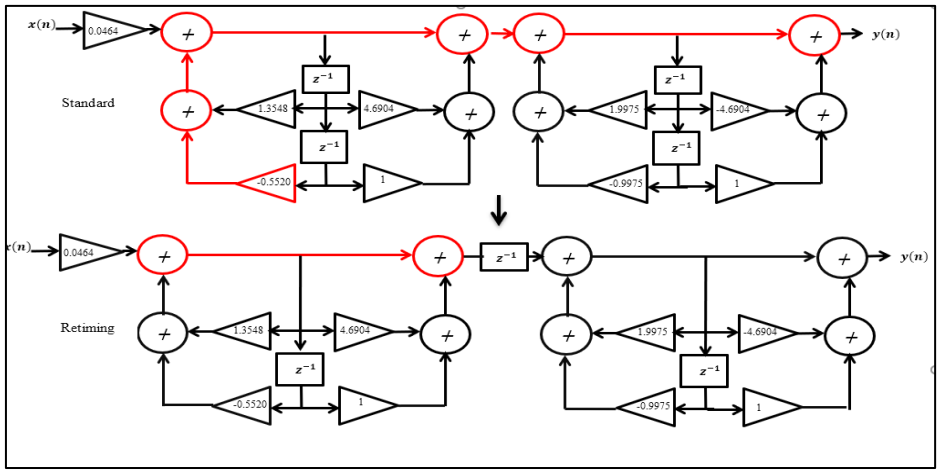
To achieve a bandpass filter using various structures, the direct form can be directly implemented from Eq. (2).

For cascaded and parallel structures, the transfer function is transformed in Eqs. (2), (3), and (4) respectively. In the case of lattice ladder realization, the coefficients are represented as shown in Eq. (5). Figures 1(a)-(d) illustrate the implementation of the bandpass filter using different structures (direct, cascaded, parallel, and lattice ladder) for both standard and retimed techniques.

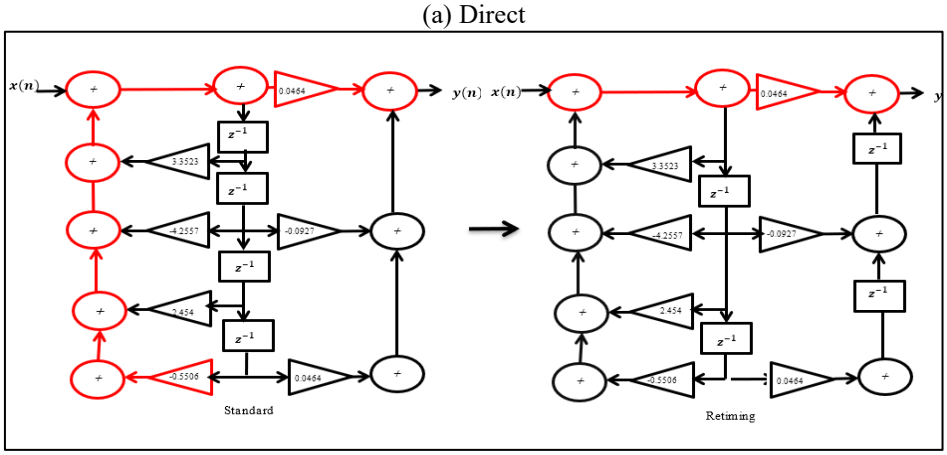
$$H[z] = 0.0464 \times \frac{1 + 4.6904z^{-1} + z^{-2}}{1 - 1.3548z^{-1} + 0.552z^{-2}} \times \frac{1 - 4.6904z^{-1} + z^{-2}}{1 - 1.39975z^{-1} + 0.9975z^{-2}} \quad (3)$$

$$H[z] = 0.0842 + \frac{-9.6786 + 7.8843z^{-1}}{1 - 1.3548z^{-1} + 0.552z^{-2}} + \frac{9.6408 - 13.8733z^{-1}}{1 - 1.9975z^{-1} + 0.9975z^{-2}} \quad (4)$$

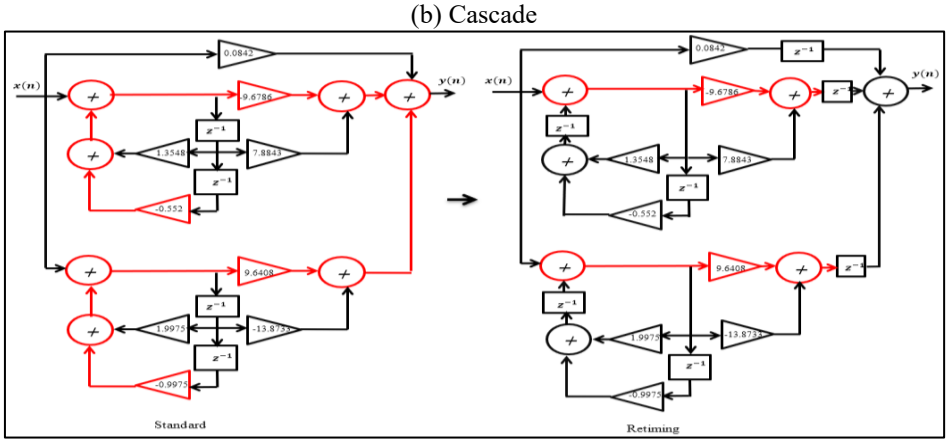
$$K1 = -1, \mathrm{K2} = 0.994, \mathrm{K3} = -0.8728, \mathrm{K} = 0.5506$$
$$C0 = -0.8345, \mathrm{C1} = -1.6688, \mathrm{C2} = -0.6782, \quad (5)$$
$$\mathrm{C3} = 0.1554, \mathrm{C4} = 0.0464$$



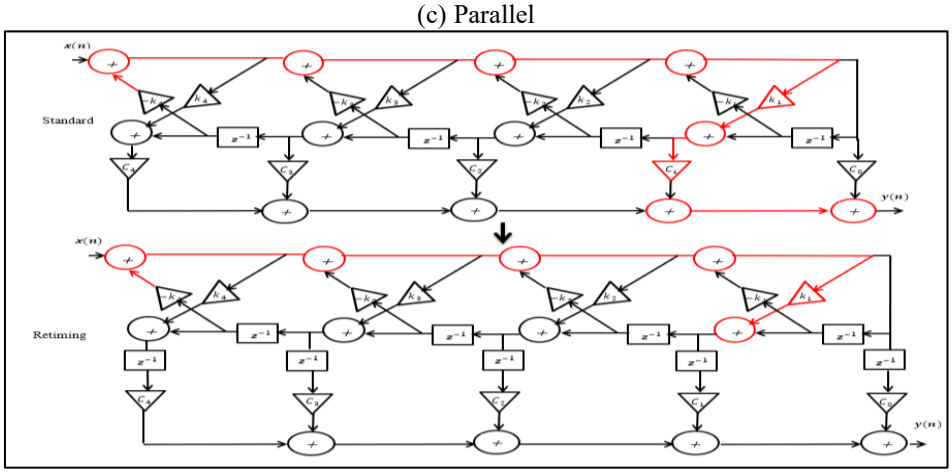
(a) Direct



(b) Cascade



(c) Parallel



(d) Lattice Ladder

Figure 1. Realization of ECG denoising system with different structures (standard & retiming)

4. RESULTS AND DISSCUTION

This section describes the hardware implementation of IIR filter structure for ECG denoising on FPGA platform. In addition, the comparison with some of related works will be presented.

4.1 FPGA implementation of IIR structures for ECG denoising

In the MATLAB environment, the XSG tool is used to define the denoising filter's transfer function, and Xilinx ISE Design Suite 14.7 is used for synthesis. The target platform for implementing these architectures is the Artix 7 (XC7A100t-1CSG324) FPGA board. The proposed IIR filter has been synthesized employing various structures; Figures 2(a)-(d) include direct, cascaded, parallel, and lattice ladders for standard technique, while the retiming technique is illustrated for the same structures in Figures 3(a)-(d). Subsequently, the generated bit streams are loaded onto the reconfigurable FPGA device. The time-domain response of the distorted ECG signal, which get from MIT-BIH Arrhythmia Database [27], and its matching filtered output are shown in Figure 4. Furthermore, the compilation report provides valuable insights into hardware utilization metrics, such as the number of slices, number of Look-Up Tables (LUTs), peak memory consumption, max frequency (MHz), the total CPU time required for XST, and total real-time to XST. These metrics are displayed in Figures 5(a)-(f), respectively. The comparison results show that the number of slices registered in four types of structures is constant for standard realization, but it increases in retiming realization, so the maximum value is found in a parallel structure. standard less than retiming by (6.6%,5.7%,3.4%,4.4%) in direct, cascade, parralel, and lattice ladder respectivlly. The LUT flip flop increased in retiming compared with standard but cascaded, which decreased, standard less than retiming by (9.2%,3.49%,4.46%)in direct, parralel, and lattice ladder but greater than in cascade by 11%.

Also, total real-time XST completion increased except for direct, which decreased, so that standard less than retiming by (6.6%, 4.7%, 7%) in cascade, parralel, and lattice ladder but greater than in direct by 25%.

It can be noticed that the maximum frequency increased in direct, cascaded realization but the frequency remained the same or close to it in parallel and lattice ladder, standard less than retiming by (8.5%,6.5%,9.9%) in direct, cascade, parralel, but greater than in lattice ladder by 0.08% . Table 2 displays a comparison between the retimed and standard structures in terms of estimated CPD. Notably, all the retimed structures exhibit a reduction in critical path delay when compared to the standard structures.

A comparative analysis of hardware utilization metrics are presented, including the number of slices, Look-Up Tables (LUTs), memory usage, and operating frequency, for various filter structures implemented using both standard and retiming techniques. This investigation revealed that a number of the tradeoffs were noteworthy, which necessitates an exhaustive discourse.

On the one hand, the manuscript highlighted that postponing the implementation time criteria rather than the standard implementation often resulted in LUT and slice metrics increases. However, in different cases which varied the filter structure, the impact was not the same. For instance, the retiming in the parallel structures produced a large rise in the slice utilization because, unlike basic structures, the parallel nature of architecture needs additional resources that the nature of retiming takes to be implemented. In the case where parallel tasks are temporalized (i.e. retiming) in the cascade structure, however, a reduction in slice utilization is observed suggesting efficient distribution of resources at this configuration level.

Furthermore, using resources fairness metric was challenged by another trade-off in operating frequency. Through the process of retiming, the delay of critical path which should also lead to the increased frequency of the maximum achievable operating frequency had been shown as the case with most of the filter structures in question although this improvement was achieved at the expense of higher resource usage. This trade-off highlights that resources have to be multiple with how systems will perform which should be considered while boding an FPGA-based system design.

Hence, the problem is multi-faceted, as balancing between resources metrics and memory use is often the main problems of filter organizations in FPGA implementation. Such as in the case where retiming is purposed to drag out paths and so reduce critical path delay but it might also greatly increase usage of memory because of the extra storage requirements for retiming registers. Therefore, this means that trade-offs are to be handled very carefully because the design constraints and optimization strategies which are aimed at scoring high on these two aspects should be well understood.

Table 2. Estimated CPD for a fourth-order IIR filter

CPD (ns)	Cascade	Direct	Parallel	Lattice Ladder
Original	60	70	60	100
Retimed	30	30	30	30

4.2 Comparative study

Table 3. Comparison of the proposed structures with references structures

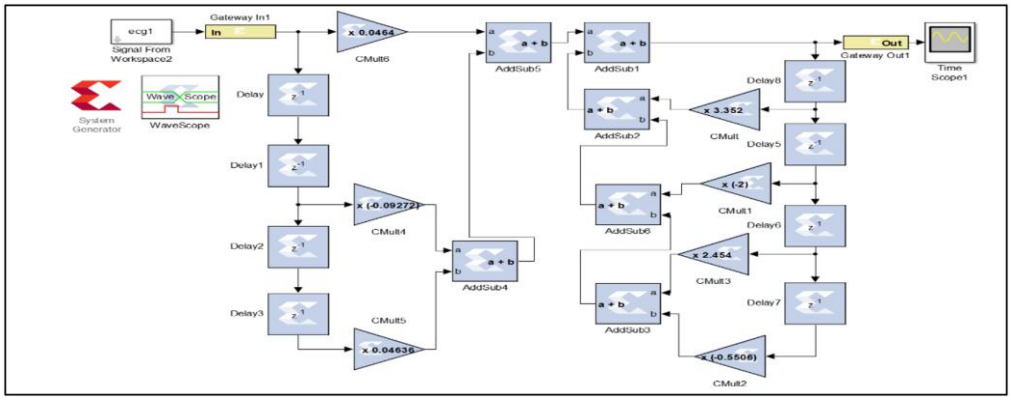
Ref. No	Filter Type	Order	FPGA Type
[17]	Low pass filter	5	N/A*
[21]	Elliptic LPF	2	Spartan 3
[20]	Notch/Antinotch	2	Zynq
[23]	Elliptic BPF	9	Virtex
Our work	BPF	4	Artix 7

N/A*: Not Available

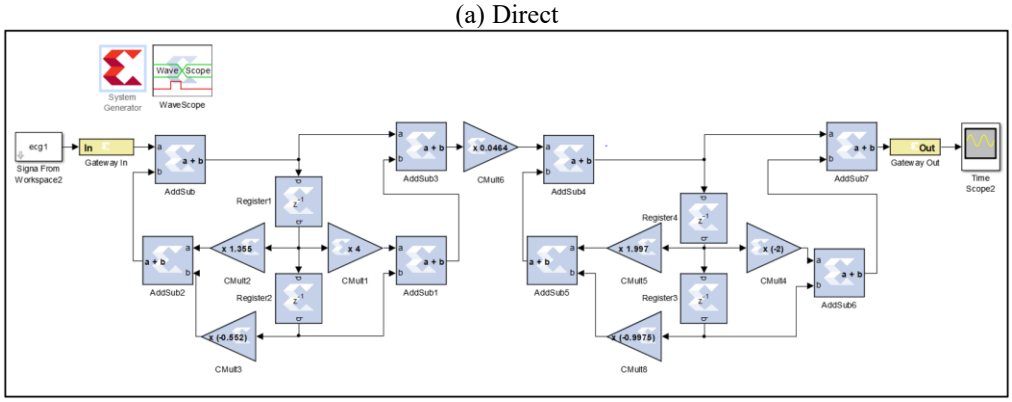
In this comparison, structures suggested in this paper are compared to those discussed in [17, 18, 21, 23] taking into account the parameterizing point of view such as filter type, order, FPGA kit type and application points as shown in Table 3. One characteristic distinction is that the filter order differs. In study [23], the presented structure had a 9th order bandpass filter, in contrast to earlier work, in which they suggested a 4th order bandpass filter. This reveals that the designed filter achieves the wanted filtering characters with fewer lags, thus possibly leading to a reduction in the computational complexity. On the other hand, as illustrated in Figure 5, it is also indicated that the suggested structures needed fewer slices for them to be developed as well as compared to those in study [23]. This fact may be read at meaning that FPGAs filter operation is more efficient and suitable, which allows to use its resources in a better way. In conclusions the parallels between the proposed approaches are emphasized concerning the filter arrangement, resources drains, and effectiveness. The

proven facts strongly suggests the remark that the proposed structures have the highest and best efficiency compare with those [17, 18, 21, 23].

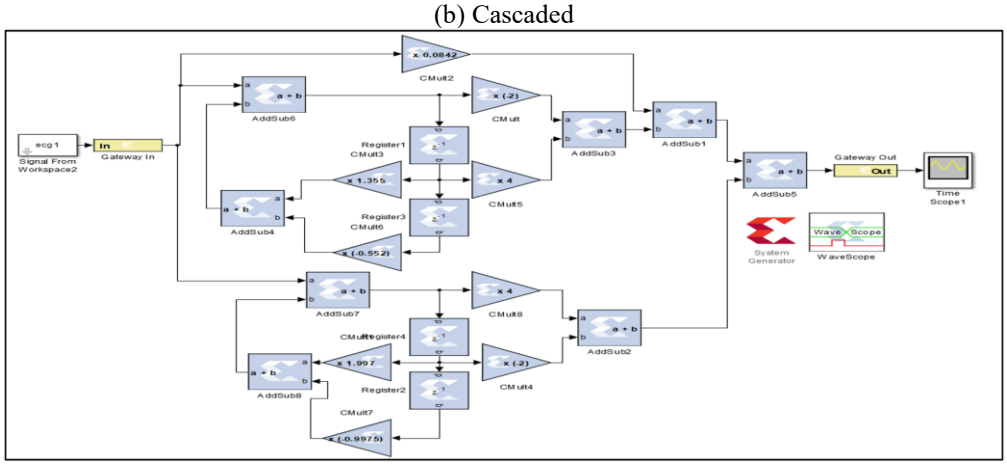
Briefly, the analysis outcome that the role of the tradeoffs involved with the resource utilization metric, memory usage and operating frequency when a structure for the FPGA filter is being designed. In which these tradeoffs have a profound influence on the design as well as performance of the provided system leading to system optimization and should be taken into consideration as a deliberate step for this purpose.



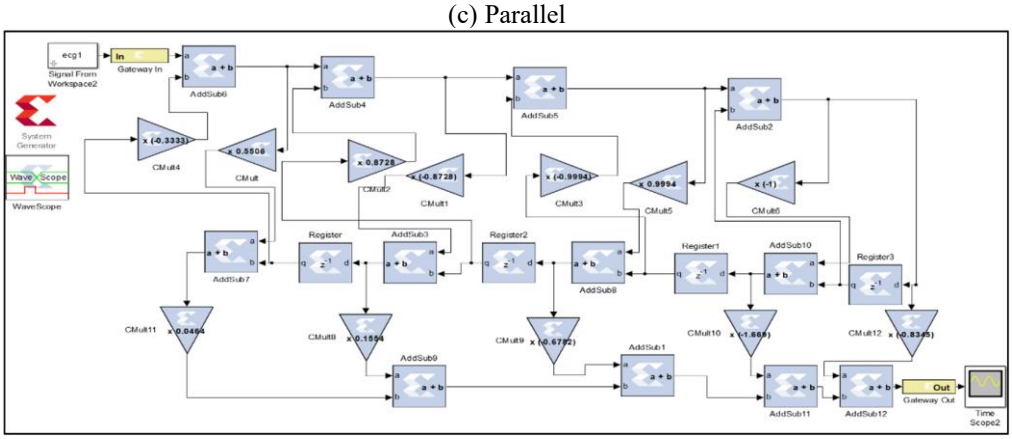
(a) Direct



(b) Cascaded

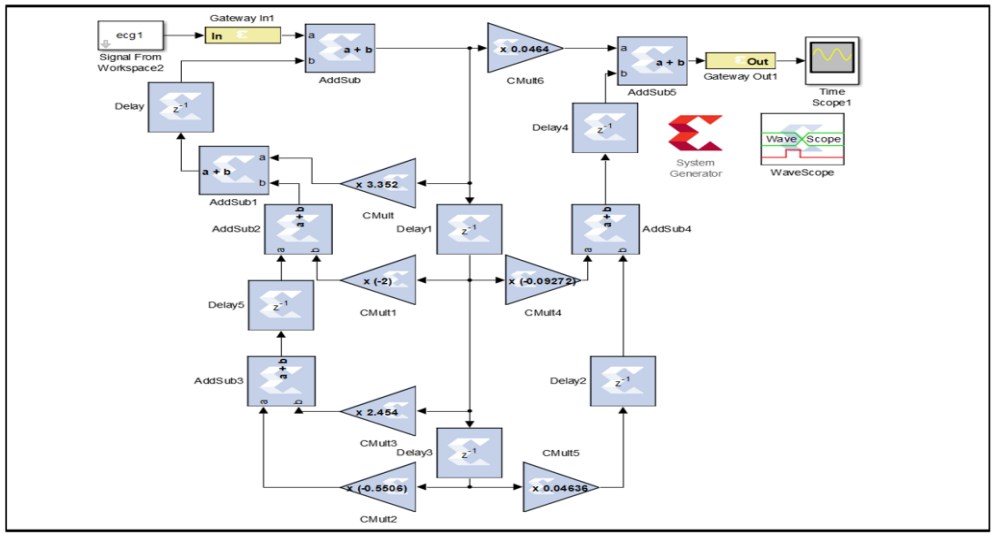


(c) Parallel

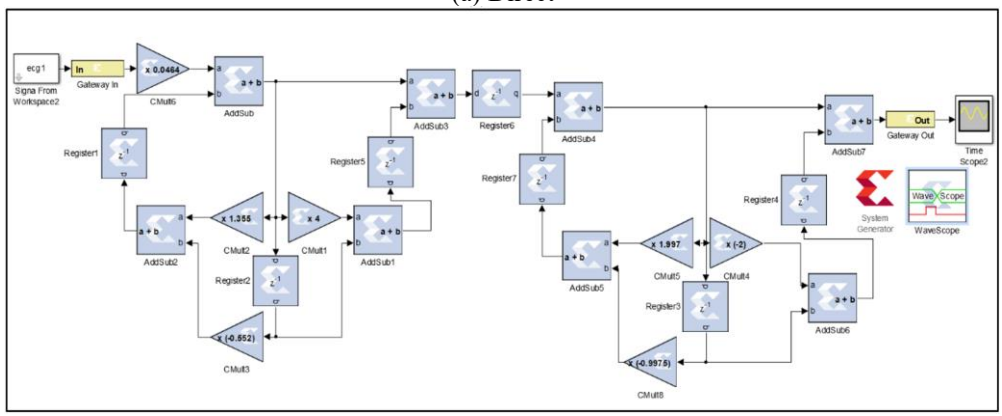


(d) Lattice ladder

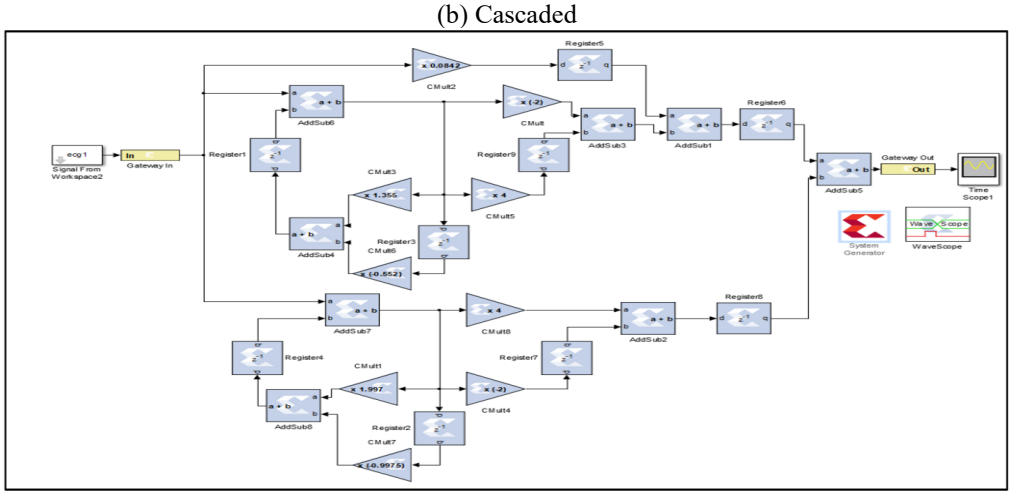
Figure 2. Hardware implementation of heart rate detection (standard techniques)



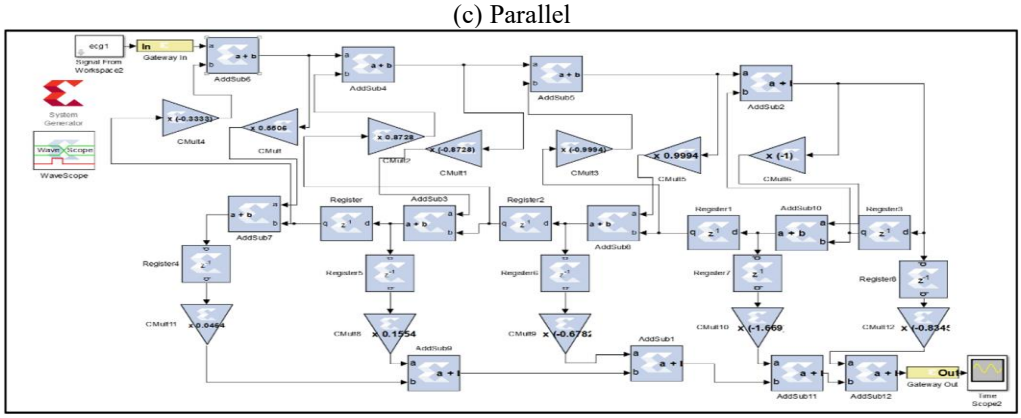
(a) Direct



(b) Cascaded



(c) Parallel



(d) Lattice ladder

Figure 3. Hardware implementation of heart rate detection (retiming techniques)

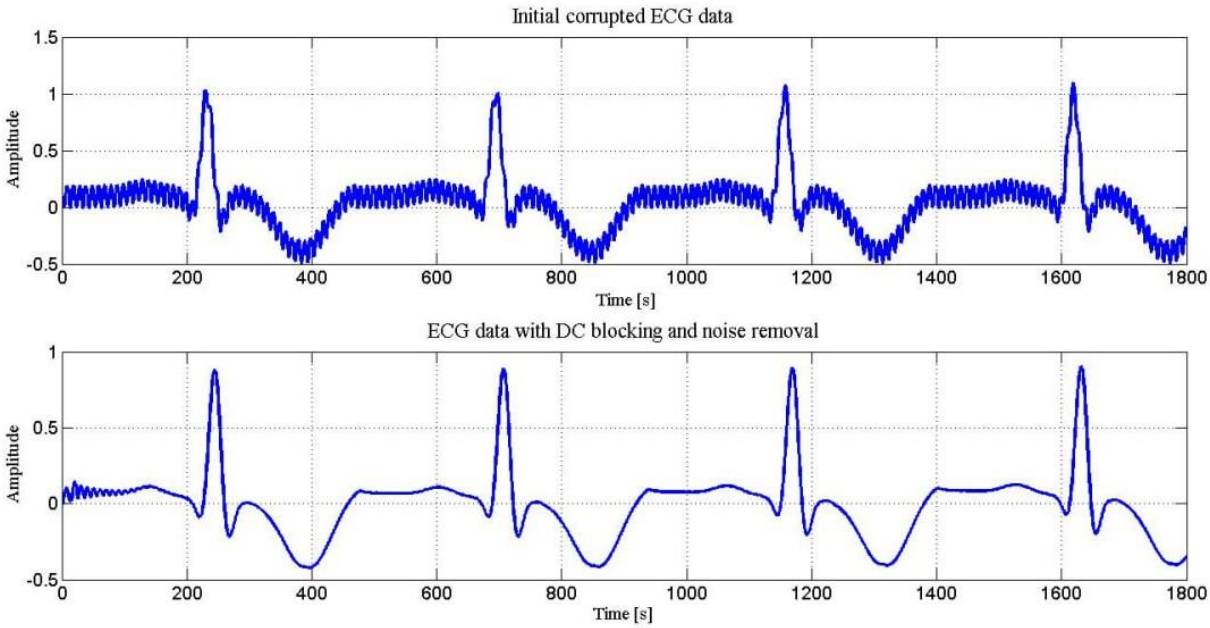
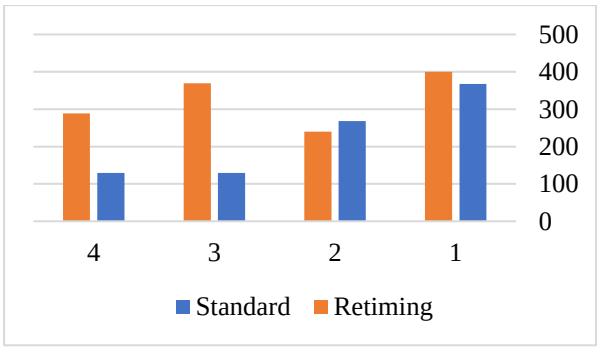
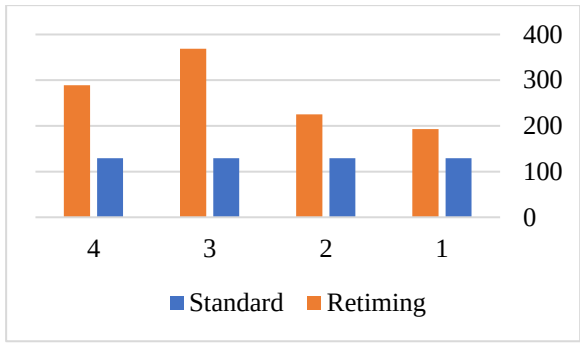


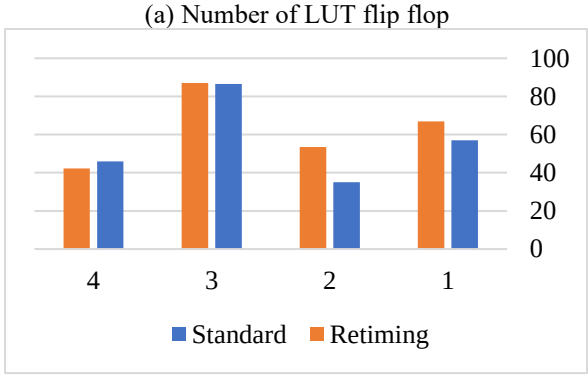
Figure 4. The time domain response of corrupted ECG signal and its filtered output



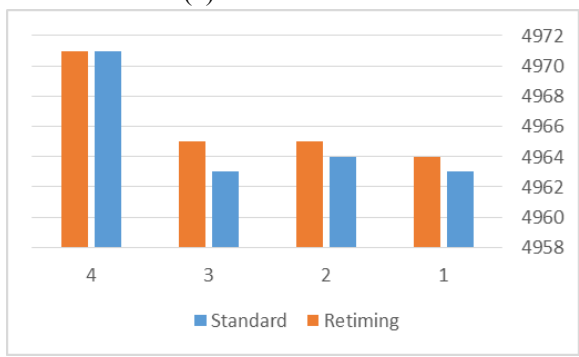
(a) Number of LUT flip flop



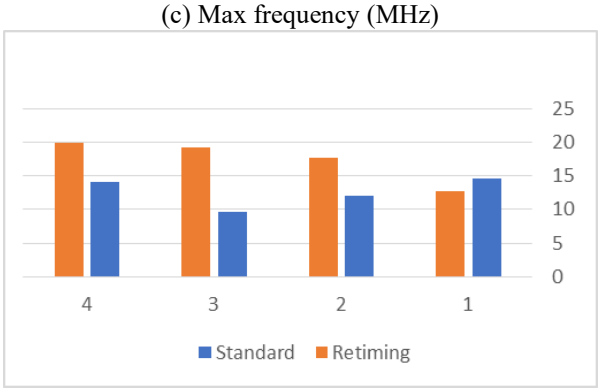
(b) Number of slices



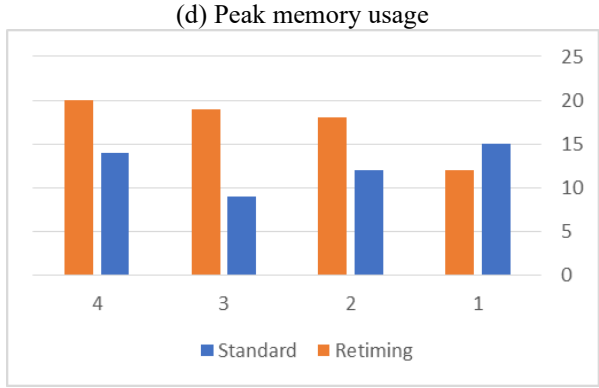
(c) Max frequency (MHz)



(d) Peak memory usage



(e) Total CPU time to XST



(f) Total Real time to XST

Figure 5. Device utilization summary of IIR filter structures

5. CONCLUSIONS

This paper will consider the possibilities of IIR filters in ECG enhancement systems and the various configurations which can be used to achieve the desired parameters. A proposed structures is constructed through the use of standard and retiming realizations, and it is analyzed according to resource utilization, a working frequency and a space memory requirement. Simulation of the bandpass filter for ECG enhancement system is performed at MATLAB (Xilinx System Generator) and synthesized by ISE Xilinx software version 14.7 on Artix7 FPGA (XC7A100t-1CSG324). In terms of slice usage, the overlapped and single-stage realization used more slices than the cascaded, and lattice stage implementation, but the five configurations have uniform slice yields. Computation in systolic and direct form were faster than MII in terms of real time and total CPU time compared with that occured in the standard realization. The most high frequency is got by an implementation of the parallel processing. The percolation box consumes the highest amount of RAM that drops to the lowest RAM used by a direct form. After all, the mentioned content was covering several IIR digital filter configurations and the practicability of that system in the ECG enhancement application. It gave an insight into the sound trade-offs of a specific filter structure in terms of resource utilization throughput, frequency of operation, and occupied memory. The implication is that the results can be a useful aid to design engineers and researchers working in the field of ECG signal processing and digital filter design. Moreover, the implications of implementing IIR digital filter structures for ECG noise reduction can be investigated, which will boost higher performance and effective ECG noise removal and enhancement. This method can encompass, the designing and testing of diverse IIR filter types like Butterworth and Elliptic among others to see how they work. Study can be carried out to find out how they affect system's performance and vice versa, optimal values for design. Adaptive IIR filters can be considered as a new generation of algorithms to choose the better parameters for filtered noise in real-time situation based on their estimation.

REFERENCES

[1] Zhu, X.Y., Basten, T., Geilen, M., Stuijk, S. (2012). Efficient retiming of multirate DSP algorithms. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 31(6): 831-844. https://doi.org/10.1109/TCAD.2011.2182352

[2] Proakis, J.G. (2007). Digital signal processing: Principles, algorithms, and applications, 4/E. Pearson Education India.

[3] Mitra, S.K., Kuo, Y. (2006). Digital signal processing: A computer-based approach (Vol. 2). New York: McGraw-Hill Higher Education.

[4] Priya, P., Ashok, S. (2018). IIR digital filter design using Xilinx system generator for FPGA implementation. In 2018 International Conference on Communication and Signal Processing (ICCSP), Chennai, India, pp. 0054-0057. https://doi.org/10.1109/ICCSP.2018.8524520

[5] Reddy, V.V., Neelaveni, M., Sandeep, M., Ahmad, S.K., Krishna, P.V. (2023). Comparison of FIR and IIR filters using ECG signal with different sampling frequencies. International Research Journal of Modernization in Engineering Technology and Science, 5(4): 2576-2581.

[6] Ariunaa, K., Tudevdagva, U., Hussai, M. (2023). FPGA based digital filter design for faster operations. Journal of VLSI Circuits and Systems, 5(2): 56-62. https://doi.org/10.31838/jvcs/05.02.09

[7] Meyer-Baese, U., Meyer-Baese, U. (2007). Digital signal processing with field programmable gate arrays (Vol. 65). Signals and Communication Technology, https://doi.org/10.1007/978-3-642-45309-0

[8] Tan, L., Jiang, J. (2018). Digital signal processing: Fundamentals and applications. Academic press.

[9] Bui, N.T., Phan, D.T., Nguyen, T.P., Hoang, G., Choi, J., Bui, Q.C., Oh, J. (2020). Real-time filtering and ECG signal processing based on dual-core digital signal controller system. IEEE Sensors Journal, 20(12): 6492-6503. https://doi.org/10.1109/JSEN.2020.2975006

[10] Ko, H.J., Tsai, J.J. (2020). Robust and computationally efficient digital IIR filter synthesis and stability analysis under finite precision implementations. IEEE Transactions on Signal Processing, 68: 1807-1822. https://doi.org/10.1109/TSP.2020.2977848

[11] Parhi, K.K. (2007). VLSI digital signal processing systems: Design and implementation. John Wiley & Sons.

[12] Ruiz-Rosero, J., Ramirez-Gonzalez, G., Khanna, R. (2019). Field programmable gate array applications—A scientometric review. Computation, 7(4): 63. https://doi.org/10.3390/computation7040063

[13] DA-Based Reconfigurable, F.I.R. (2014). Efficient FPGA and ASIC realizations of DA-based reconfigurable FIR digital filter. IEEE Transactions on Circuits and Systems II: Express Briefs, 61: 511-515.

[14] Gadawe, N.T., Fathi, T.A., Qaddoori, S.L., Hamad, R.W. (2021). Synthesis and implementation of IIR filter using VHDL language. IOP Conference Series: Materials Science and Engineering, 1152(1): 012026. https://doi.org/10.1088/1757-899X/1152/1/012026

[15] Woods, R., McAllister, J., Lightbody, G., Yi, Y. (2008). FPGA-based implementation of signal processing systems. John Wiley & Sons.

[16] Meher, P.K. (2015). On efficient retiming of fixed-point circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 24(4): 1257-1265. https://doi.org/10.1109/TVLSI.2015.2453324

[17] Bujjibabu, P., Sravani, N. (2017). Architecture based performance evaluation of IIR digital filters for DSP applications. In 2017 International Conference on Big Data Analytics and Computational Intelligence (ICBDAC), Chirala, Andhra Pradesh, India, pp. 224-229. https://doi.org/10.1109/ICBDACI.2017.8070838

[18] Pathak, V., Nanda, S.J., Joshi, A.M., Sahu, S.S. (2018). High speed implementation of Notch/Anti-notch IIR filter on FPGA. In 2018 15th IEEE India Council International Conference (INDICON), Coimbatore, India, pp. 1-6. https://doi.org/10.1109/INDICON45594.2018.8986985

[19] Seshadri, R., Ramakrishnan, S. (2021). FPGA implementation of fast digital FIR and IIR filters. Concurrency and Computation: Practice and Experience, 33(3): e5246. https://doi.org/10.1002/cpe.5246

[20] Datta, D., Dutta, H.S. (2021). High performance IIR filter implementation on FPGA. Journal of Electrical Systems and Information Technology, 8: 1-9. https://doi.org/10.1186/s43067-020-00025-4

[21] Gaikwad, K.M., Chavan, M. (2018). Elliptic filter

implementation using Xilinx system generator for processing of ECG signal. Communications on Applied Electronics, 7(12): 25-29. https://doi.org/10.5120/cae2018652743
[22] Mukherjee, P., Bakshi, A. (2020). FPGA based system to remove noise from ECG signal. International Journal of Information Technology and Electrical Engineering, 9.
[23] Ladekar, M.Y., Joshi, Y.V., Manthalkar, R.R. (2021). Performance analysis in higher-order IIR Filter structures with application to EEG signal. Circuits, Systems, and Signal Processing, 40(8): 4047-4063. https://doi.org/10.1007/s00034-021-01662-4
[24] Ravi, R.V., Subramaniam, K., Roshini, T.V., Muthusamy, S.P.B., Prasanna Venkatesan, G.K.D. (2019). Optimization algorithms, an effective tool for the design of digital filters: A review. Journal of Ambient Intelligence and Humanized Computing, 1-17. https://doi.org/10.1007/s12652-019-01431-x
[25] Jibon, R.H., Podder, E., Bulbul, A.A.M., Bairagi, R.N., Ahmed, M.S., Shohagh, I.A. (2018). Performance analysis of IIR filter in removing PLI from EEG signal. International Journal of Engineering & Technology, 7(4): 5363-5367. https://doi.org/10.14419/ijet.v7i4.26715
[26] Dallalbashi, Z.E. (2020). MatLab based design and implemetation of digita filter. IJCSNS International Journal of Computer Science and Network Security, 20(1): 95.
[27] Moody, G., Mark, R. (2005). MIT-BIH Arrhythmia Database. https://physionet.org/content/mitdb/1.0.0/.

NOMENCLATURE

Ta	computation time of adder
Tm	computation time of multiplier
N	order of the filter
P1	N/2 No. of cascaded sections.
P2	No. of parallel sections.
b	pertain to the zeros
a	pertain to the poles