

Enhancing Data Communication Performance: A Comprehensive Review and Evaluation of LDPC Decoder Architectures



Maryam Imad Subhi^{1*}, Qusay Al-Doori¹, Omar Alani²

¹ Control and System Engineering Department, University of Technology, Baghdad 10066, Iraq

² School of Science, Engineering, and Environment, University of Salford Manchester, Salford M5 4WT, UK

Corresponding Author Email: cse.21.09@grad.uotechnology.edu.iq

<https://doi.org/10.18280/isi.280501>

ABSTRACT

Received: 20 July 2023

Revised: 15 September 2023

Accepted: 13 October 2023

Available online: 31 October 2023

Keywords:

Error Correction Codes (ECC), Field Programmable Gate Array (FPGA), Low-Density Parity-Check codes decoding algorithms, Low-Density Parity-Check codes (encoder/decoder), Parity Check Matrix (PCM)

Error Correction Codes (ECCs) stand as a linchpin in ensuring data accuracy in wireless communication. As the landscape of modern communication standards continues to expand, there is a mounting inclination towards efficient ECC technologies, such as Low-Density Parity-Check codes (LDPCs). Distinguished by their near-capacity performance and low computational complexity, LDPCs are increasingly utilized in the successful encoding and decoding of data. This study undertakes an exploration of recent advancements in LDPC research, encompassing the analysis of decoding algorithms, architectures, applications, simulations, real-world implementations, and complexities across various hardware platforms. The central research problem addressed within this work is the identification of the most efficacious LDPC decoder implementation, with an emphasis placed on Field-Programmable Gate Array (FPGA) technology. From the outcomes of this study, the Min-Sum algorithm emerged as the favored choice for LDPC decoding, particularly within FPGA implementations. The selection of this algorithm is attributable to its simplicity and implementation feasibility, thus directly addressing the posed research problem. The inherent simplicity of the Min-Sum algorithm's structure renders it a practical choice for real-world applications. Further, its proficiency in error correction and compatibility with FPGA hardware underscore its potential for augmenting the reliability of data transmission in communication systems. The findings of this study advocate for the Min-Sum algorithm as a valuable asset in LDPC decoding, notably within FPGA implementations. This positions it as a promising candidate for optimizing data communication systems. The selection of FPGA as the implementation platform reaffirms its practicality and relevance in contemporary communication technology, thus offering a comprehensive solution to the identified research problem.

1. INTRODUCTION

The burgeoning development of digital wireless communication and information technology predicates the necessity for an effective communication system—one that excels in capacity, speed, cost, lossless data transfer, and secure communication. Channel coding, a subject of rising prominence in communication, is integral to this objective. The application of channel coding techniques bolsters the reliability of communication systems by attenuating errors in the received data. The inclusion of additional bits in the transmitted data facilitates the detection and correction of errors by the receiver [1].

Among the myriad techniques employed for error correction, low-density parity-check (LDPC) codes have been delineated as a notably promising solution. Constituting the class of Error-Correcting Codes (ECC), LDPC codes have garnered substantial attention due to their impressive performance near the Shannon limit and computational efficiency [2]. Although originally conceived by Robert Gallager in 1962, the complexity of LDPC codes initially rendered them unsuitable for simulation and real-world implementation, leading to their dormancy for several decades [2]. The resurgence of interest in LDPC codes occurred in

1996, following their rediscovery by Mackay and Neal [3], which precipitated a surge in research endeavors [4, 5].

Several characteristics of LDPC codes render them apt for high-throughput and real-time applications:

(1) Due to their exceptional error correction capacity, which closely approximates the theoretical limit set by Shannon's channel coding theorem, LDPC codes have been widely adopted across diverse wireless communication standards.

(2) The codes can be efficiently decoded using parallel iterative decoding algorithms with low latency [6, 7].

LDPC codes have found applications in various communication systems, including Wi-Fi [8], WiMAX [9, 10], 5G New Radio (NR), and DVB-S2 [11, 12]. Additionally, they have been utilized in the CV-QKD system and NAND memory storage [13, 14].

When compared to other codes like turbo codes [15], LDPC codes possess several advantages such as a straightforward code structure and a fully parallelizable decoding implementation [16]. The high throughput of LDPC codes offers several benefits, including improved performance for larger block lengths, increased adaptability, simplified demonstration and theoretical verification, reduced decoding complexity, and rapid decoding [17, 18]. Furthermore, LDPC codes outperform the Bose-Chaudhuri-Hocquenghem (BCH)

and Reed-Solomon (RS) methods for longer code word lengths, providing superior error correction performance [19].

This paper seeks to conduct an exhaustive review of recent literature on LDPC decoding algorithms, architectures, applications, simulation methodologies, and real-world implementations. The primary research objective is to identify the optimal LDPC decoder implementation approach, with a particular focus on Field Programmable Gate Array (FPGA) technology.

The remainder of this paper is structured as follows: Section 2 presents and critically evaluates recent studies. Section 3 introduces various types and structures of LDPC codes and discusses their advantages. Section 4 provides an overview of LDPC decoder types, their architectures, and the strengths and weaknesses of LDPC decoder algorithms. Section 5 outlines the design criteria of the LDPC decoder and discusses its advantages and challenges. Finally, Section 6 and the conclusion cover open issues and concerns related to the LDPC decoder.

2. RELATED WORK

An extensive body of literature exists on the topic of LDPC decoding approaches and their implementation, underscoring their significance in the realm of communication systems. The implementation of these codes on Field Programmable Gate Array (FPGA) devices exhibits considerable variation, stemming from factors such as algorithm type, LDPC type, and specific implementation objectives. These objectives can range from enhancing performance and reducing complexity to increasing throughput.

Upon reviewing the existing literature, several prominent types of LDPC decoder algorithms emerge:

- (1) The Min-Sum decoding algorithm and its associated significance.
- (2) The architecture of parallel layout decoding.
- (3) The semi-parallel LDPC decoding architecture.

These types and their related studies are explored in the ensuing discussion.

In recent years, a comprehensive survey was conducted by Shao et al. [20], wherein a detailed analysis of Turbo, LDPC (Low-Density Parity Check), and Polar decoder Application-Specific Integrated Circuit (ASIC) implementations was performed. The examination of these coding schemes focused on their use in cellular communication systems, with a particular emphasis on the transition from Turbo to LDPC and Polar codes in 5G New Radio (NR) data and control channels.

A myriad of factors was considered in the evaluation, drawing from ASIC implementations across assorted sources. These factors included computational complexity, volume, error correction capability, flexibility, area efficiency, and energy efficiency. Moreover, it was established that LDPC codes outperformed Bose-Chaudhuri-Hocquenghem (BCH) and Reed-Solomon (RS) algorithms for extended codeword lengths, exhibiting a robustness and parallelism superior to Hamming, Reed-Solomon, and Reed-Muller codes in high-bit error rate scenarios [21].

In comparison to turbo codes [22], LDPC codes demonstrated superior performance with considerable block lengths, offering flexibility, ease of theoretical verification, and practical implementation. They exhibited reduced complexity, efficient computation, support for parallel processing, and high throughput for swift decoding processes. These characteristics underscore the potential and

applicability of LDPC codes in contemporary communication systems.

The prominence of LDPC decoding algorithms, most notably the soft decision and min-sum algorithms, is largely attributable to their demonstrable effectiveness and precision in error correction. In an investigation undertaken by Hussein et al., an evaluation of soft decision decoding algorithms' performance for LDPC codes on Additive White Gaussian Noise (AWGN) channels was conducted, with the Bit Error Rate (BER) as the primary focus. The Min-Sum algorithm was found to surpass other algorithms in a range of circumstances, delivering superior results [23].

In a comprehensive literature review by Roberts and Anguraj, LDPC decoding algorithms and their applications were meticulously examined and classified based on various criteria, including performance, similarities, scalability, numerical stability, and hardware feasibility. A comparative study by Zhou et al. pitted several methods against each other—BF, WBF, BP, and LLR—to ascertain the top-performing algorithm through a performance analysis of LDPC decoding algorithms. Their findings suggested that the NMS algorithm outperformed the others, showcasing lower complexity and superior performance [24-26].

These studies collectively offer invaluable insights into the performance of LDPC decoding algorithms and their practical applications.

A number of research efforts have been directed towards enhancing the hardware efficiency, throughput, and error correction of LDPC decoding algorithms. In one such study, an Offset Min-Sum (OMS) algorithm for a hardware-efficient Quasi-Cyclic LDPC (QC-LDPC) decoder was proposed, which achieved high throughput. However, this study also underscored the significant developmental costs associated with high-throughput LDPC decoders [27].

In another investigation, the throughput and hardware usage efficiency for regular and irregular LDPC codes were augmented using the Minimum-Sum (MS) algorithm on the base matrix (BG1) of the 5G standards. It was noted that while more iterations improved error correction, they concomitantly increased the decoding time [28].

In a different study, LDPC codes and the Min-Sum algorithm were implemented in a Differential Chaos Shift Keying (DCSK) communication system, resulting in improved BER performance and real-time processing efficiency on a Xilinx Kintex7 FPGA platform [29].

These studies collectively contribute to the advancement of LDPC decoding algorithms, augmenting hardware efficiency and BER performance. However, they simultaneously draw attention to the challenges posed by development costs and increased decoding time for high-throughput LDPC decoders and iterative processes.

Several studies have been embarked upon to refine LDPC decoding techniques applicable to a variety of communication systems. In one such investigation [30], the smOMS algorithm was employed to optimize Min-Sum decoding for irregular 5G NR LDPC codes. This technique was found to reduce hardware requirements and effectively manage the Signal-to-Noise Ratio (SNR) dips caused by the irregularity of 5G NR codes. The same study also highlighted the potential of partial parallel LDPC to improve 5G NR Bit Error Rate (BER).

In the study of Liu et al. [31], the Threshold-Attenuated Min-Sum Algorithm (TAMSA) was adapted for a (155, 64) QC-Tanner code LDPC decoder. This approach was observed to augment the BER without necessitating additional hardware.

The layered TAMSA was introduced as a cost-effective solution with superior hardware capabilities. The suitability of LDPC for 5G NR was scrutinized in this study, with a particular emphasis on error correction.

Further, the potential of a high-speed, low-complexity LDPC decoder employing the SAMS algorithm was explored [32]. This decoder was capable of achieving a throughput of 10.5 Gb/s while sustaining an acceptable Bit Error Rate (BER). It addressed the challenges of routing congestion and power utilization and was designed specifically for millimeter-wave 60-GHz systems, outperforming previous designs.

Additional contributions to the understanding and development of LDPC coding techniques were made in two pivotal studies [33, 34]. One of these studies conducted an evaluation of LDPC code designs on FPGA devices, focusing on adaptability, processing speed, and parallelism. The study classified critical factors in FPGA-based LDPC decoder design, underlining the distinctions between LDPC code designs and their performance characteristics. Another comprehensive review of recent advancements in LDPC decoding algorithms was undertaken, discussing their role in error control coding and highlighting both algorithm-driven and hardware-realization-based approaches.

Several studies have ventured into the domain of FPGA-based LDPC decoder designs for diverse LDPC codes and communication standards. In the study of Likhobabin et al. [35], a highly parallel decoder that leverages Min-Sum decoding was proposed. This decoder demonstrated a throughput of up to 500 Mbps for QC-LDPC codes under the DVB-S2X standard. Nevertheless, it was challenged by long code words and large matrices.

A subsequent work centered on 5G QC-LDPC codes and introduced a highly parallel and adaptable decoder architecture that achieved a processing rate of 10 GB/s [36]. However, the flexibility of the architecture imposed certain limitations on hardware design. An additional study utilized FPGA-based parallel layered decoding with adaptive normalization for 5G NR LDPC codes [37]. While it offered remarkable scalability for varying lifting factors and enhanced decoder BER performance, it was observed to potentially experience reduced throughput with minor lifting factor values. These designs collectively aimed to strike a balance between high throughput and hardware constraints, catering to a variety of code configurations and matrix sizes.

Further strategies to enhance LDPC encoding and decoding techniques were proposed in subsequent studies [38-40]. One such investigation proposed a high-throughput IR-QC-LDPC encoding and decoding method that utilized a normalized min-

sum algorithm (NMSA), achieving a decoding throughput of 27.85 Mbps when implemented on an FPGA. The conversion of quasi-cyclic LDPC codes into block quasi-cyclic LDPC codes was also explored, resulting in an impressive throughput of 2.97 Gbps after five iterations on the FPGA. Another study demonstrated an FPGA implementation of a low-complexity regular LDPC decoder capable of achieving a high data rate with low latency.

In the realm of LDPC codes, numerous significant contributions have been made, leading to a broad spectrum of applications across varied domains. Exploration of their potential for the forthcoming generation of IoT networks has been undertaken. For instance, a Dual Min-Sum (DMS) architecture for LDPC codes in the context of IEEE 802.16e was introduced [41], which exhibited superior error correction performance.

Attention was also directed towards LDPC decoders for Wi-Fi in another study of Tsatsaragkos and Paliouras [42], where effective decoding algorithms and interconnection techniques were established for achieving high throughput. Additionally, a serial LDPC decoder that accomplished substantial speedups on a System-on-Chip platform was presented [43, 44]. This was particularly evident at low signal-to-noise ratios. The same study also demonstrated the use of a DE1-SoC FPGA-based information transceiver board for LDPC coding, achieving minimal errors and an impeccable 0% error rate during data transmission through UART serial communication.

Moreover, a semi-parallel LDPC decoding architecture was proposed [45], which amplified throughput for solid-state drives, albeit at the expense of increased hardware overhead. These studies collectively offer valuable insights into the design and optimization of LDPC decoding for various applications and code types.

The tables provided contain comprehensive information on a plethora of studies pertaining to LDPC codes. Table 1 primarily focuses on recent research conducted in the field, including the authors, year, and research concept. Conversely, Table 2 ventures into an in-depth exploration of different types and methods of LDPC codes, their implementation approaches, and the challenges encountered in recent times. Specific LDPC code constructions, employed decoding algorithms, and performance analysis under various channel conditions may also be included in the table. Furthermore, it encompasses the advantages and drawbacks of the LDPC codes.

Overall, these studies and tables provide a rich tapestry of research in the field of LDPC codes, enhancing our understanding of their potential and the challenges associated with their implementation in various contexts.

Table 1. Studies reviewed in the last few years

References	Year	Research Concept(s)
[34]	2021	This paper provides a comprehensive and systematic exploration of the latest developments in LDPC decoding algorithms. Additionally, it includes a comprehensive evaluation and analysis of various notable LDPC decoding strategies.
[33]	2021	This study aims to assess the efficacy of LDPC code designs on Field-Programmable Gate Array (FPGA) devices through a case study. The evaluation takes into account the diverse attributes of these devices, including their adaptability, high processing speed, and parallel processing capabilities.
[23]	2021	Presented compares the bit error rate (BER) performance of soft decision decoding algorithms based on the LDPC wireless communication system.
[24]	2020	A survey of recent developments in LDPC decoding algorithms and some of their practical applications are presented. Different LDPC decoding algorithms are analyzed and compared in detail regarding their performance, similarities, scalability, numerical stability, and hardware realizability.
[25]	2020	A performance analysis of the LDPC decoding algorithm is presented. by contrasting BF, WBF, BP, and BP algorithm performance with LLR, MS, and NMS algorithm performance.
[20]	2019	Presented "A Survey of Turbo, LDPC, and Polar Decoder ASIC Implementations" and used the LDPC family of codes for eMBB data and polar codes for eMBB commands.

Table 2. The LDPC type and method, implementation method and challenges in the last few years

References	Year	LDPC TYPE	Method	Implementation	Advantage	Challenges/Drawbacks
[27]	2023	The QC-LDPC decoder's design is parallel and optimized for hardware performance.	Offset min-sum (OMS) decoding algorithm	Field-programmable gate array (Xilinx Zynq-Ultrascale+ board)	The decoder under consideration exhibits a throughput that is 7.5 times greater and a hardware efficiency that surpasses the state-of-the-art implementation by 34%.	LDPC decoders exhibit a remarkably high decoding throughput performance; nonetheless, it is important to note that they are accompanied by a substantial development cost.
[35]	2022	QC-LDPC	Using a layered design and a Min-Sum decoding algorithm	A highly parallel FPGA implementation	Any LDPC codec is supported by the DVB-S2X standard. This architecture is small in size and has a high throughput	The complexity of LDPC decoding in the context of the DVB-S2X standard is attributed to the considerable length of the code words and the substantial size of the associated parity-check matrices.
[28]	2022	Regular and irregular LDPC codes	HUE and throughput are enhanced by implementing a Minimum-Sum (MS) algorithm on the 5G base matrix (BG1).	FPGA	Both throughput and HUE can be enhanced by including more look-up tables (LUTs) and flip-flops (FF).	When the iteration is increased, the BER/FER performance improves. Decoding does take longer when there are more iterations involved, though.
[36]	2021	5G QC-LDPC	Highly parallel and flexible hardware architecture	FPGA	The decoder features high processing throughput and flexibility to support all 5G configurations.	This outstanding performance imposes difficult constraints on the hardware design.
[29]	2021	LDPC code	Min-Sum algorithm	Kit Xilinx kintex7 FPGA	The proposed system model greatly improves the BER and the real-time process.	The suggested algorithm's hardware co-simulation results for the user data and recovery information demonstrate a delay caused by the extraction process's operation and some Xilinx blocks.
[41]	2021	IEEE802.16e LDPC codes with code rates of 0.5 and 0.75 and a block length of 2304	Dual min-sum (DMS) architecture	6-bit CMOS standard	The proposed methodology demonstrates exceptional error correction capabilities in terms of both bit error rate (BER) and block error rate (BLER).	Excludes power consumption.
[37]	2020	5G NR LDPC codes	Layered scheduling in parallel, with a customized interlayer network and an ensuing method of adaptive normalization	FPGA	Allows for excellent scalability for variable lifting factors and increases decoder BER performance.	The small lifting factor values implemented in the decoder are the main drawback. This reduces the decoder's throughput.
[30]	2020	Irregular 5G NR LDPC codes	Single-minimum offset min-sum (smOMS) algorithm	FPGA	The reduced-complexity offset min-sum decoding can be achieved using partially parallel LDPC.	The significant drop in SNR performance Because of the extreme irregularity of 5G NR codes, the weight parameter is selected separately for check nodes with various check node weights. The SNR performance loss is largely mitigated by using this technique.
[31]	2020	(155,64) QC-Tanner code	Threshold-attenuated min-sum algorithm, a layered TAMSA architecture, a full-parallel computing structure	A Xilinx Kintex 7 FPGA. The power consumption and area were determined using a Cadence SOC. Process.	The threshold-attenuated MSA algorithm improved BER performance over the standard AMSA algorithm without adding any extra hardware. A layered TAMSA architecture was proposed to reduce the hardware cost.	A semi-parallel decoding strategy is a highly advantageous choice for QC-LDPC codes due to its ability to provide excellent throughput performance and meet hardware requirements effectively. This architectural design commonly presents a favorable balance between hardware complexity and decoding throughput.

[38]	2019	IR-QC-LDPC	A parallel cyclic shift structure, A normalized min-sum algorithm (NMSA)	FPGA, Simulation by MATLAB.	Realizing a high throughput, decoding can achieve 183.36 Mbps when the code rate is 5/6, while the throughput can achieve 27.85 Mbps when the code rate is 2/3.	The NMSA, when compared to the SPA, can significantly reduce decoding complexity while introducing significant performance degradation in the form of bit error rate (BER).
[32]	2019	Binary LDPC code	Second minimum approximation min-sum algorithm.	IEEE802.11ad, row-based layer scheduling, 28-nm 1P9M CMOS process	Achieves high throughput at the expense of acceptable BER degradation for practical applications.	The number of iterations slightly increased.
[21]	2018	QC-LDPC	Probabilistic GaB (PGaB) algorithm	Xilinx Virtex-6 (FPGA)	GaB's decoding performance was greatly improved, and the gap between GaB and other hard decision bit flipping decoding algorithms was closed. Simulation results showed that the probabilistic GaB now has better decoding performance than the GDBF.	Soft-decision algorithms offer high error-correction performance.
[46]	2018	LDPC Code	A generalized algorithmic method of constructing NPU's that support run-time flexibility	Altera Stratix IV EP4SGX530 FPGA	In this case, for an IEEE 802.11n LDPC decoder, the proposed architecture offers improvement in hardware efficiency compared to the best of these two benchmarks	The complex interconnection worsens the timing, which may cause a synchronous digital system to fail. Also, it occupies more hardware resources.
[39]	2018	(8176, 7154) LDPC code, QC-LDPC	Converts a quasi-cyclic LDPC code to a block quasi-cyclic LDPC code.	Simulation with MATLAB and FPGA, and then writing a Verilog hardware program for testing and analysis	After five iterations, they get a throughput of 2.97 GB/s by making the encoder and decoder more parallel and giving them high throughput.	The simple implementation of these LDPC encoders has a high storage and computation overhead.
[42]	2018	WiFi and other communication standards support a variety of quasi-cyclic LDPC codes with different codeword lengths and code rates.	Changes are made to the MS algorithm similar to how the log-SP algorithm works when decoding.	Simulation by MATLAB, simulations via FPGA designed in VHDL, and mapped into the Virtex7-XC7VX485T FPGA (VC707 evaluation board) using the Xilinx design flow	In terms of throughput and space requirement, the Wi-Fi LDPC decoder architecture outperformed state-of-the-art decoders.	Higher frequency usually necessitates more power consumption.
[43]	2018	Regular LDPC codes	Min-Sum Algorithm (MSA)	Serial LDPC decoder implementation on a System-on-Chip platform with a CPU and a Field Programmable Gate Array (FPGA)	When the signal-to-noise ratio (SNR) is low, any gains in performance are magnified. The speedups of the suggested design are up to 8.11 and 2.79, respectively, compared to a non-optimized hardware decoder and a software decoder.	A serial decoder's poor speed is one of its biggest drawbacks. Optimization strategies, including array partitioning, loop unrolling, pipelining, and fixed-point conversion, are used to solve these problems.
[40]	2017	(3, 4) Regular LDPC code	(Belief propagation) simplified "Min-Sum"	VHDL and implemented on the FPGA circuit	The high data rate, low latency, and low complexity are all features of the design. The BER versus SNR can be improved by making the code bigger while keeping the same parallelism principle.	The SPA has better BER performance when compared to the MSA.
[45]	2017	0.94, length 35840, quasi-cyclic LDPC code	An LDPC decoding scheme that uses a semi-parallel layout.	Xilinx VC709 FPGA	Enhance the error correction coding throughput for high-performance solid-state drives.	The increased throughput comes at the expense of increased hardware overhead.

3. LDPC PARITY CHECK MATRIX (PCM)

The Parity Check Matrix (PCM) is pivotal in LDPC codes, significantly affecting their error correction capability and computational complexity. The PCM's structure is denoted as an $(M \times N)$ matrix, where M represents the number of parity-check equations and N represents the total number of bits. This matrix defines the code rate (R), calculated as $R = K/N$, where $K=N - M$. This establishes the relationship between information bits and parity-check bits within the code. The defining feature of LDPC codes is the sparsity of their PCM, meaning that in a well-designed code, the number of ones (non-zero elements) in the PCM is lower than the number of zeros. LDPC codes' error-correction performance greatly relies on the structure of their parity-check matrix (PCM). Properly constructed PCMs with an optimal distribution of ones and zeros can exhibit exceptional error-correcting capabilities, even at low code rates. For instance, concentrating 1s in specific PCM areas for satellite communication can mitigate predictable noise patterns, though it may complicate decoding. Conversely, a uniform 1 distribution simplifies decoding and handles variable noise conditions more effectively. This highlights the significance of PCM design in tailoring LDPC codes for specific applications, making research on LDPC PCM design and implementation a prominent topic [1].

Tanner graphs are a common graphical representation used for LDPC codes [47]. These graphs consist of two types of nodes: variable nodes, representing individual bits within the codeword, and check nodes, representing the parity-check equations. The connections between variable and check nodes in the Tanner graph are depicted as edges directly derived from the elements in the Parity Check Matrix, as illustrated in Figure 1.

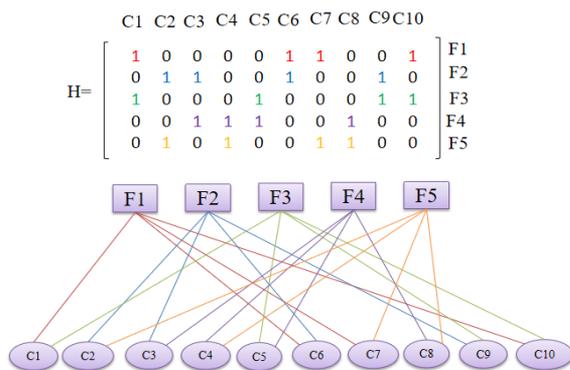


Figure 1. Illustrates the LDPC representation in both matrix and graph forms, referred to as the Tanner graph. In this representation, the check nodes are denoted by rows (F1, F2, F3, F4, F5), while the variable nodes are represented by columns (c1-c10)

LDPC codes are classified into binary and non-binary (NB-LDPC) categories depending on their Parity Check Matrix (PCM) characteristics. Binary LDPC codes are further subdivided into two types: regular and irregular. An LDPC code is designated as regular when both column and row weights are uniform; otherwise, it falls into the irregular category [48]. Gallager's LDPC code is constructed in a regular manner by randomly selecting positions for 1s with fixed integers in each row and column. For moderate code lengths, NB-LDPC codes can exhibit superior error-correcting

capabilities compared to binary LDPC codes. However, this improved error correction capability comes at the cost of higher decoding complexity. For larger block lengths, binary LDPC codes have the advantage of improved error correction and channel capacity. In high-throughput communication systems aiming for minimal errors and fast data rates, binary LDPC codes with their regular structure are preferred, as seen in Wi-Fi and large-scale applications like satellite communication and data storage. In contrast, non-binary LDPC codes shine in scenarios requiring low error floors or customized code rates, offering superior performance in shorter code lengths, suitable for applications like optical communication and digital video broadcasting [49, 50].

3.1 The LDPC encoder

LDPC encoders are an essential component of the LDPC code system, which converts a message signal into an encoded message using a PCM. The LDPC encoder generates parity-check bits based on the message bits and the parity-check matrix. The encoder's primary goal is to create a codeword with a low density of ones, allowing for efficient decoding with minimal errors because the decoding efficiency of LDPC codes is closely tied to the codeword structure, specifically the distribution of ones and zeros inside the codewords. The sparsity of ones in a codeword decreases the number of parity-check equations that involve them. Consequently, the processing requirements during the decoding process are lowered, resulting in a much faster decoding procedure. LDPC codes use iterative message-passing methods like belief propagation or sum-product to correct errors. When codewords have few ones, these algorithms excel at error detection and correction due to reduced ambiguity in the parity-check equations [51, 52].

LDPC encoding commences with the setup of a generator matrix (G) and a parity-check matrix (H), where G is systematically derived from H , and these matrices possess specific attributes based on the LDPC code design. Creating a sparse parity-check matrix (H) marks the initial phase, strategically placing 1s within it and profoundly influencing the encoding process. Subsequently, the generator matrix (G), usually exhibiting sparsity, is formed through the transposition of matrix A from H , playing a pivotal role in codeword generation. The H matrix then undergoes Gauss-Jordan elimination to attain a row-reduced echelon form, eliminating redundancy and ensuring efficiency. The encoding operation itself involves generating codewords (C) by modulo-2 multiplication of message bits with the generator matrix G , akin to exclusive-OR operations. Each resulting codeword comprises a combination of informational and redundant bits, a matrix multiplication product.

In addition, the Gauss-Jordan elimination method, a widely recognized mathematical technique employed in diverse disciplines such as linear algebra and coding theory, is utilized in LDPC codes to modify the parity-check matrix (H). The process entails a series of row operations to convert the matrix into a simplified row-reduced echelon form, enhancing computational efficiency in LDPC encoding. The approach of this method encompasses fundamental operations such as row swapping, row scaling, and row addition/subtraction to strategically rearrange the parity-check matrix (H) to optimize the positioning of '1s'. The functionality of an LDPC encoder and decoder in channel coding is illustrated in Figure 2 [53, 54].

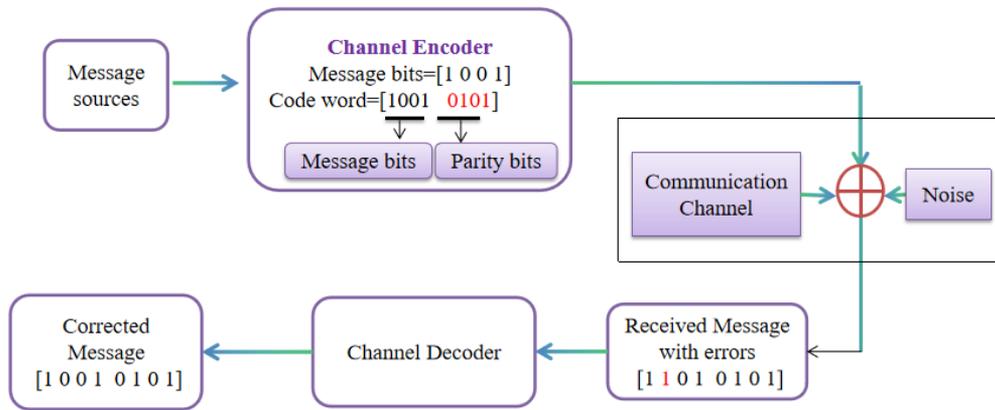


Figure 2. Illustrates a functional LDPC encoder and decoder employed in the context of channel coding

3.2 The LDPC decoder

LDPC decoding is a critical process in error correction for various communication systems. It involves extracting the original message from a noisy transmission by applying a decoding algorithm to the received signal. The field of LDPC decoding has garnered considerable interest owing to its capacity to attain performance close to the Shannon capacity and its compatibility with hardware implementation. This process typically involves using the PCM to perform iterative decoding of the received signal until the original message is obtained. LDPC decoders can be categorized based on their decoding algorithms, hardware implementation, and the number of iterations necessary to attain satisfactory error rates [2].

LDPC decoding involves an iterative procedure that relies on the Tanner graph to fulfill parity check conditions. The received codeword is considered valid when its resemblance to the transmitted codeword is verified. Messages are transmitted between nodes via the edges of the Tanner graph during the LDPC decoding process. The term "message-passing algorithm" is commonly used to describe this group of decoding algorithms [55]. Each node in a Tanner graph functions independently, with data available only along the edges connecting them. These decoding algorithms call for the messages to be relayed between nodes a predetermined number of times or until the desired result is reached. This class of algorithms is also known as an iterative algorithm [56].

In general, LDPC decoding is a computationally intensive process, and the complexity increases with the number of iterations required to achieve the desired error correction level. However, a strong LDPC code can reduce the number of iterations needed, thereby improving processing efficiency while maintaining high transmission efficiency. In addition, energy consumption is a critical consideration in the design of an LDPC decoder, as high energy dissipation can lead to reliability issues and increased costs. Compared to LDPC encoding, decoding is more challenging since the decoder has to consider all possible code words in the message simultaneously. Therefore, developing efficient decoding algorithms is essential for realizing the full potential of LDPC codes in various applications [3].

4. TYPES OF LDPC DECODERS AND ARCHITECTURE

LDPC decoders play a pivotal role in modern

communication systems. They are essential for ensuring data's reliable and error-free transmission in a wide range of applications. In this discussion, we will explore LDPC decoder implementation, decoding algorithms, and architectural aspects:

4.1 LDPC decoder implementation

The LDPC decoder architecture is a critical component of communication systems, but its effectiveness hinges on proper implementation. This entails meticulous design and configuration to ensure it functions optimally for error correction. The choice of hardware, such as field-programmable gate arrays (FPGAs), plays a pivotal role in achieving efficient LDPC decoding. Field-programmable gate arrays are a crucial technology used in LDPC decoder implementation. They offer the advantage of reconfigurability, enabling them to be tailored to the specific requirements of LDPC decoding. They are highly efficient for parallel processing and essential for handling large amounts of data in real-time, a common requirement in communication systems.

Additionally, LDPC decoding's throughput and complexity are influenced by factors such as codeword length in bits, code rate (the ratio of information bits to codeword length), computation complexity at each processing node, interconnection complexity, and the number of local computation iterations. Achieving a balance between decoder performance, complexity, and speed is crucial [57, 58].

4.2 Decoding algorithms

LDPC decoding algorithms typically function by employing either hard decisions (e.g., bit flipping, BF) or soft decisions (e.g., sum-product, SP, and min-sum, MS) using incoming messages from the noisy channel, as illustrated in Figure 3 [59]. Better bit error rate (BER) performance can be achieved with soft decision decoding algorithms, which take as input the channel probabilities expressed as a logarithmic ratio, also referred to as a log-likelihood ratio (LLR), however, hard decision-decoding algorithms, are simple and fast, and their hardware implementations are easy [60]. The following is an elucidation of some algorithms utilized in LDPC decoding:

The bit-flip (BF) algorithm is a hard, decision-oriented decoding approach. Once the encoded message from the channel is received, a binary decision is made and sent to the decoder. When it comes to implementing algorithms in hardware, the bit-flip algorithm is the most straightforward

because of the simplicity of its check nodes and variables. However, the algorithm has low BER performance because it employs a hard-decision approach, making binary choices based on received channel data and oversimplifying the information by not considering the probabilities associated with different bit values. This binary decision-making can lead to incorrect bit flips in noisy channel conditions, resulting in higher decoding errors. In contrast, soft-decision algorithms use log-likelihood ratios (LLRs) for a more nuanced representation of bit likelihood, making them more accurate in noisy conditions due to their ability to make probabilistic judgements about transmitted bits [61].

4.2.1 Variable node operation for BF

$$V_n \begin{cases} 0 & \text{If majority}(C_i) = 0 \\ 1 & \text{If majority}(C_i) = 1 \\ V_n & \text{Otherwise} \end{cases} \quad (1)$$

where, $n= 1, 2, \dots, N$ (variable nodes).
 $i= 1, 2, \dots, dv$ (degree of variable node "n")

4.2.2 Check node operation for BF

$$C_k = V_1 \oplus V_2 \oplus \dots \oplus V_l \quad \forall l \neq k \quad (2)$$

where, $l, k= 1, 2, \dots, dc$ (degree of check node)
 The Sum of Products Algorithm (SPA) is a soft decision message-passing algorithm that involves LLR (intrinsic message) variable node operations to facilitate decoding decisions. Eq. (3) illustrates the transmission of LLRs to variable nodes for decoding. The input LLRs are summed at the v-nodes, and the resulting computed (extrinsic) messages are communicated to the c-nodes via the connected edges (C). The function of the check nodes (C) is denoted by equation (4). The corresponding variable nodes receive the output messages. Check nodes also do parity checks. This process is repeated until the maximum number of iterations has been reached or the parity test has been passed.

The Sum of Products Algorithm (SPA) offers excellent decoding performance is primarily attributed to its soft decision-making capabilities, iterative processing, and adaptability, which allow it to handle noisy channels and provide accurate error correction effectively [62]. However, it does come with its share of challenges and drawbacks. These can include computational complexity due to the nonlinear

operations performed at the check nodes, which can be resource-intensive and time-consuming. Additionally, transmitting high-precision extraneous messages between nodes requires significant computational effort. These factors contribute to the algorithm's computational load and can impact its real-time processing capabilities, making it less suitable for applications where low latency is crucial. Moreover, while the SPA provides high-quality error correction, it may not be the most power-efficient solution, making it less ideal for energy-constrained devices.

4.2.3 Variable node operation for SPA

$$V_i = LLR_n + \sum_{j \neq i} C_j \quad (3)$$

where, $i, j = 1, 2, \dots, dv$ (degree of variable node "n").

4.2.4 Check node operation for SPA

$$C_k = 2 \tanh^{-1} \left(\prod_{l \neq k} \tanh \frac{V_l}{2} \right) \quad (4)$$

where, $l, k = 1, 2, \dots, dc$ (degree of check node).
 The Min-Sum Algorithm (MSA) is a simplification of the SPA. As shown in Eq. (5), the check node operation is streamlined to simplify the algorithm. The MSA is easy to implement in hardware because it uses simple math and logic operations.

On the other hand, quantizing the soft input messages greatly affects how well the algorithm works [63]. There are many MS algorithm variants, such as "offset min-sum" [64], "normalized min-sum" [65], and "adaptive quantization in min-sum" [66]. To boost the MS algorithm's BER performance, these alterations are proposed.

4.2.5 Check node operation for MSA

$$C_k = \prod_{l \neq k} \text{sign}(V_l) \times \min_{l \neq k} |V_l| \quad (5)$$

where, $l, k = 1, 2, \dots, dc$ (degree of check node).
 Layered decoders are often used in the LDPC because they can do calculations quickly and are built consistently [67]. Vertically stacked decoding and horizontally layered decoding are two types of layered decoding schemes.

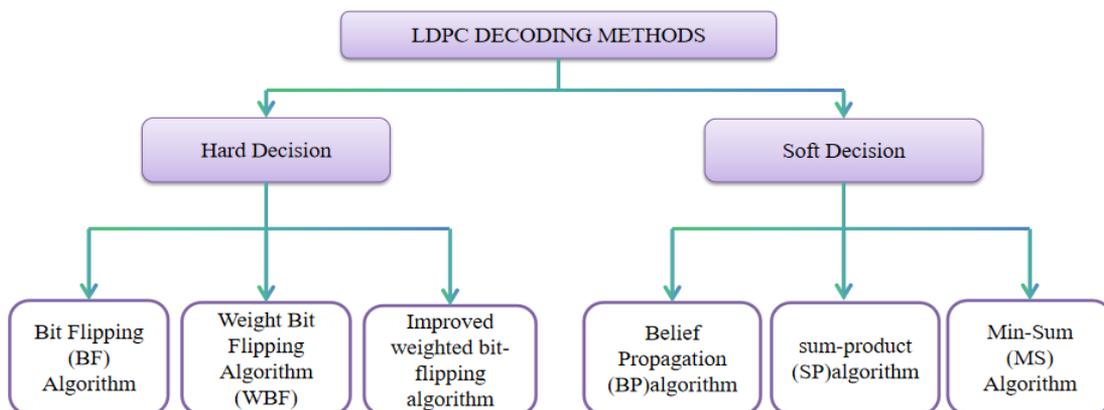


Figure 3. Types of LDPC decoding algorithms

4.3 LDPC decoder architectures

There are several types of architectures associated with LDPC decoder design, including:

(1) Parallel: This architecture provides exceptionally low power dissipation and great throughput but is inefficient in the area [68].

(2) Serial: The parallel technique results in an incredibly complicated interconnection challenge. A sequential decoding machine is used to avoid this issue, which processes the input nodes in a linear order from the first bit-node to the last in each iteration [69].

(3) Semi-parallel: The semi-parallel decoding design provides a better combination of throughput performance and hardware requirements, making it an excellent choice for QC-LDPC codes. This type of architecture generally delivers a fair trade-off between hardware complexity and decoding throughput [70].

(4) Minimum semi-parallel: This architectural design exemplifies the disparity in performance and complexity between semi-parallel and serial decoders. The architecture demonstrates commendable suitability and proficiency in accommodating high-performance applications, particularly those that impose significant demands on wireless and mobile systems as well as portable devices. One of the primary difficulties associated with Low-Density Parity-Check (LDPC) codes pertains to their pragmatic application [71].

5. DESIGN CRITERIA AND PERFORMANCE OF LDPC DECODERS

An LDPC decoder is an essential component of any system utilizing LDPC codes, as it is responsible for detecting and correcting errors in incoming data. As such, it is important to consider certain design criteria when designing an LDPC decoder. The primary criterion for the design of an LDPC decoder is its efficacy in error correction. The coding rate, which refers to the ratio of information bits to total bits in a codeword, plays a crucial role in determining the error correction capabilities of an LDPC decoder. The more efficient the decoder, the higher the code rate. For example, satellite communication systems, where challenging channel conditions, often caused by signal interference, necessitate using a highly effective LDPC decoder featuring a high code rate to correct errors effectively and ensure reliable data transmission.

In addition to code rate, the degree distributions of the LDPC code are vital as they dictate the decoder's performance. The degree distributions within LDPC codes, affecting the number of connections for each variable and check node, wield a substantial influence on both error correction performance and computational complexity; for instance, a high-degree distribution might be chosen for robust error correction in wireless communication, while a lower-degree distribution could be preferred for real-time applications like video streaming to achieve lower complexity and faster decoding. One other crucial criterion is the LDPC decoder's complexity. The number of steps needed to decode a codeword is used to measure complexity. The lower the complexity, the better for system performance. This complexity can be reduced using iterative decoding algorithms, which can decode multiple codewords in parallel [72, 73].

The implementation complexity of an LDPC decoder is also

important when designing one. This complexity is determined by the hardware architecture used. It can be reduced by using dedicated hardware blocks such as FPGAs [74, 75] or ASICs because these specialized hardware components are designed to perform LDPC decoding tasks efficiently and in parallel, offloading the computational burden from the general-purpose processor and thus reducing overall complexity. Finally, it is important to consider power consumption when designing an LDPC decoder. Low power consumption ensures that the decoder will not consume too much power and can operate in low-power environments such as mobile devices or embedded systems. Low power consumption can be achieved using low-power hardware architectures such as FPGAs or ASICs and optimizing the decoding algorithm [76-79].

6. ADVANTAGES AND CHALLENGES OF LDPC DECODER

The main challenge of LDPC decoders is their complexity. LDPC decoders require much computing power to decode messages, making them difficult to implement in real-time applications such as wireless communication in cellular networks, autonomous vehicles relying on real-time data processing, and platforms offering live video streaming, where LDPC's computational demands can strain processing resources and cause latency issues.

Additionally, the codes used by LDPC decoders are often very long, making them difficult to store and transmit. Nevertheless, the main advantage of LDPC decoders is their accuracy. LDPC decoders can detect and correct errors with high accuracy, making them ideal for applications where data integrity is essential. For instance, in satellite communication systems. Furthermore, LDPC decoders can effectively detect errors in data corrupted by noise or interference, making them well-suited for use in noisy environments by iteratively exchanging messages between check nodes and variable nodes in a graphical representation, making probabilistic judgments about bit values through log-likelihood ratios (LLRs), and refining these assessments until convergence or parity checks are satisfied, allowing them to offer robust error correction in such conditions. Overall, LDPC decoders are a powerful tool for improving communication reliability, but they come with challenges and advantages. While they require a large amount of computing power and can be difficult to store and transmit, they offer high levels of accuracy and are well-suited for use in noisy environments [80-82].

7. CONCLUSIONS

LDPC codes are a powerful error correction tool in various applications. The recent advances in the LDPC coding field have further increased these codes' performance and applicability. This study thoroughly examines the fundamental principles of LDPC and decoding schemes, performance measurement, comparisons, and applications for the last few years. Recent research topics include the design of low-complexity LDPC decoding, the advancement of the min-sum algorithm, and the use of LDPC codes in new fields such as the Internet of Things (IoT) and the 5G wireless communication standard.

The analysis underscores the imperative for ongoing research and empirical testing. Key computational factors,

including hardware complexity, decoding stability, overhead, and convergence rates, demand further exploration. Also, further improvements to the min-sum algorithm are needed, including measuring its power consumption, decoding speed in different implementations, and reducing implementation complexity. This quest for optimisation is crucial as it directly impacts the reliability of communication systems. Indeed, as the error correction algorithm's time increases, the reliability of the communication system decreases, underscoring the importance of finding faster error correction methods.

In addition, this paper explored modern technology, with a special focus on the implementation aspect, considering factors such as complexity and decoding time. It becomes clear that with an increase in the time required for error correction algorithms, the reliability of the communication system decreases. Therefore, pursuing ways to correct errors faster is paramount for maintaining a reliable communication system.

By its nature, increasing the speed of the decoder leads to an increase in complexity. Thus, finding a delicate balance, a trade-off between speed and complexity, is a fundamental consideration in building an ideal communication system.

REFERENCES

- [1] Morelos-Zaragoza, R.H. (2006). The art of error correcting coding. John Wiley & Sons.
- [2] Paolini, E. (2018). Low-Density Parity-Check (LDPC) Codes. In: Micheloni, R., Marelli, A., Eshghi, K. (eds) Inside Solid State Drives (SSDs), Springer Singapore, Singapore, pp. 407-453. https://doi.org/10.1007/978-981-13-0599-3_12
- [3] MacKay, D.J., Neal, R.M. (1997). Near Shannon limit performance of low density parity check codes. *Electronics Letters*, 33(6): 457-458. <https://doi.org/10.1049/el:19961141>
- [4] Majeed, A.H. (2012). LDPC error floor improvement. *Engineering Technology Journal*, 30(3): 474-488.
- [5] Mosleh, M.F. (2011). Evaluation of low density parity check codes over various channel types. *Engineering Technology Journal*, 29(5): 961-971.
- [6] Ma, X. (2007). On constructing low-density parity-check codes. University of Waterloo, Waterloo, Canada.
- [7] Abd Al-Kareem, L.G. (2011). Low-Density Parity Check (LDPC) codes for a proposed slantlet transform ofdm system in a rayleigh fading channels with perfect and pilot channel estimation for M_Ary Psk modulation. In *Engineering Conference of Control, Computers and Mechatronics*, University of Technology, Baghdad, pp. 65-78.
- [8] Brack, T., Alles, M., Lehnigk-Emden, T., Kienle, F., Wehn, N., L'Insalata, N.E., Rossi, F., Rovini, M., Fanucci, L. (2007). Low complexity LDPC code decoders for next generation standards. In *Design, Automation & Test in Europe Conference & Exhibition*, Nice, France, pp. 1-6. <https://doi.org/10.1109/DATE.2007.364613>
- [9] Gupta, S.H., Virmani, B. (2009). LDPC for Wi-Fi and WiMAX technologies. In *International Conference on Emerging Trends in Electronic and Photonic Devices and Systems*, Varanasi, India, pp. 262-265. <https://doi.org/10.1109/ELECTRO.2009.5441120>
- [10] Hameed, S.M. (2012). Planning of WiMAX networks based on modified empirical path loss model. *Journal of Communications Information Sciences*, 2(1): 16-24. <https://doi.org/10.4156/jcis.vol2.issue1.2>
- [11] Nguyen, T.T.B., Nguyen Tan, T., Lee, H. (2019). Efficient QC-LDPC encoder for 5G new radio. *Electronics*, 8(6): 668. <https://doi.org/10.3390/electronics8060668>
- [12] Dielissen, J., Hekstra, A., Berg, V. (2006). Low cost LDPC decoder for DVB-S2. In *Proceedings of the Design Automation and Test in Europe Conference*, Munich, Germany, pp. 1-6. <https://doi.org/10.1109/DATE.2006.243816>
- [13] Lin, D., Huang, D., Huang, P., Peng, J., Zeng, G. (2015). High performance reconciliation for continuous-variable quantum key distribution with LDPC code. *International Journal of Quantum Information*, 13(2): 1550010. <https://doi.org/10.1142/S0219749915500100>
- [14] Cui, L., Liu, X., Wu, F., Lu, Z., Xie, C. (2021). A low bit-width LDPC min-sum decoding scheme for NAND flash. *IEEE Transactions on Computer-Aided Design of Integrated Circuits Systems*, 41(6): 1971-1975. <https://doi.org/10.1109/TCAD.2021.3100273>
- [15] Fleah, M.A., Al-Doori, Q.F. (2019). State space parallelization method for a 16-bit turbo encoder. *Engineering Technology Journal*, 37(12): 553-557. <https://doi.org/10.30684/etj.37.12A.9>
- [16] Hou, J., Siegel, P.H., Milstein, L.B. (2001). Performance analysis and code optimization of low density parity-check codes on Rayleigh fading channels. *IEEE Journal on Selected areas in Communications*, 19(5): 924-934. <https://doi.org/10.1109/49.924876>
- [17] Richardson, T., Kudekar, S. (2018). Design of low-density parity check codes for 5G new radio. *IEEE Communications Magazine*, 56(3): 28-34. <https://doi.org/10.1109/MCOM.2018.1700839>
- [18] Ahn, S.K., Kim, K.J., Myung, S., Park, S.I., Yang, K. (2018). Comparison of low-density parity-check codes in ATSC 3.0 and 5G standards. *IEEE Transactions on Broadcasting*, 65(3): 489-495. <https://doi.org/10.1109/TBC.2018.2874541>
- [19] Zhong, H., Zhang, T. (2005). Block-LDPC: A practical LDPC coding system design approach. *IEEE Transactions on Circuits Systems I: Regular Papers*, 52(4): 766-775. <http://dx.doi.org/10.1109/TCSI.2005.844113>
- [20] Shao, S., Hailes, P., Wang, T.Y., Wu, J.Y., Maunder, R.G., Al-Hashimi, B.M., Hanzo, L. (2019). Survey of turbo, LDPC, and polar decoder ASIC implementations. *IEEE Communications Surveys Tutorials*, 21(3): 2309-2333. <https://doi.org/10.1109/COMST.2019.2893851>
- [21] Unal, B., Akoglu, A., Ghaffari, F., Vasić, B. (2018). Hardware implementation and performance analysis of resource efficient probabilistic hard decision LDPC decoders. *IEEE Transactions on Circuits Systems I: Regular Papers*, 65(9): 3074-3084. <https://doi.org/10.1109/TCSI.2018.2815008>
- [22] Fleah, M.A., Al-Doori, Q.F. (2019). Design and Implementation of Turbo encoder/decoder using FPGA. In *2019 First International Conference of Computer and Applied Sciences (CAS)*, Baghdad, Iraq, pp. 46-51. <https://doi.org/10.1109/CAS47993.2019.9075589>
- [23] Hussein, Y.M., Mutlag, A.H., Al-Nedawe, B.M. (2021). Comparisons of soft decision decoding algorithms based LDPC wireless communication system. *IOP Conference*

- Series: Materials Science and Engineering, 1105: 012039. <https://doi.org/10.1088/1757899X/1105/1/012039>
- [24] Roberts, M.K., Anguraj, P. (2021). A comparative review of recent advances in decoding algorithms for Low-Density Parity-Check (LDPC) codes and their applications. *Archives of Computational Methods in Engineering*, 28(4): 2225-2251. <https://doi.org/10.1007/s11831-020-09466-6>
- [25] Zhou, F., Niu, L., Tian, B. (2020). Performance analysis of LDPC decoding algorithm. *Journal of Physics: Conference Series*, 1453: 012026. <https://doi.org/10.1088/1742-6596/1453/1/012026>.
- [26] Hameed, S.M., Abdulsatar, S.M., Sabri, A.A. (2021). BER comparison and enhancement of different optical OFDM for VLC. *International Journal of Intelligent Engineering Systems*, 14(4): 326-336. <https://doi.org/10.22266/ijies2021.0831.29>
- [27] Verma, A., Shrestha, R. (2022). Low computational-complexity soms-algorithm and high-throughput decoder architecture for QC-LDPC codes. *IEEE Transactions on Vehicular Technology*, 72(1): 66-80. <https://doi.org/10.1109/TVT.2022.3203802>
- [28] Selvakumari, R.S. (2022). Performance analysis of Min-Sum based LDPC decoder architecture for 5G new radio standards. *Materials Today: Proceedings*, 62: 4965-4972. <https://doi.org/10.1016/j.matpr.2022.03.693>
- [29] Mosleh, M.F., Hasan, F.S., Abdulhameed, A.H. (2021). Reduce the resources utilization of LDPC decoder based on min-sum decoder for spread spectrum applications. *IOP Conference Series: Materials Science and Engineering*, 1105: 012033. <https://doi.org/10.1088/1757-899X/1105/1/012033>
- [30] Petrović, V.L., El Mezeni, D.M. (2020). Reduced-complexity offset min-sum based layered decoding for 5G LDPC codes. In *28th Telecommunications Forum (TELFOR)*, Belgrade, Serbia, pp. 1-4. <https://doi.org/10.1109/TELFOR51502.2020.9306590>
- [31] Liu, Y., Tang, W., Mitchell, D.G. (2020). Efficient implementation of a threshold modified min-sum algorithm for LDPC decoders. *IEEE Transactions on Circuits Systems II: Express Briefs*, 67(9): 1599-1603. <https://doi.org/10.1109/TCSII.2020.3001601>
- [32] Lopez, H., Chan, H.W., Chiu, K.L., Tsai, P.Y., Jou, S.J.J. (2019). A 75-Gb/s/mm² and energy-efficient LDPC decoder based on a reduced complexity second minimum approximation min-sum algorithm. *IEEE Transactions on Very Large Scale Integration Systems*, 28(4): 926-939. <https://doi.org/10.1109/TVLSI.2019.2955925>
- [33] Ashou, A.H., Alneema, D.A. (2021). FPGA hardware design of different LDPC applications: Survey. *Asian Journal of Computer Science Engineering*, 6(2): 35-44. <https://doi.org/10.22377/ajcse.v6i2.158>
- [34] Kingston Roberts, M., Kumari, S., Anguraj, P. (2021). Certain investigations on recent advances in the design of decoding algorithms using low-density parity-check codes and its applications. *International Journal of Communication Systems*, 34(8): e4765. <https://doi.org/10.1002/dac.4765>
- [35] Likhobabin, E., Ovinnikov, A., Goriushkin, R., Nikishkin, P., Khokhryakov, E. (2022). High throughput FPGA implementation of LDPC decoder architecture for DVB-S2X standard. In *International Conference on Information, Control, and Communication Technologies (ICCT)*, Astrakhan, Russian Federation, pp. 1-4. <https://doi.org/10.1109/ICCT56057.2022.9976733>
- [36] Nadal, J., Baghdadi, A. (2021). Parallel and flexible 5G LDPC decoder architecture targeting FPGA. *IEEE Transactions on Very Large Scale Integration Systems*, 29(6): 1141-1151. <https://doi.org/10.1109/TVLSI.2021.3072866>
- [37] Katyushnyj, A., Krylov, A., Rashich, A., Zhang, C., Peng, K. (2020). FPGA implementation of LDPC decoder for 5G NR with parallel layered architecture and adaptive normalization. In *IEEE International Conference on Electrical Engineering and Photonics (EExPolytech)*, St. Petersburg, Russia, pp. 34-37. <https://doi.org/10.1109/EExPolytech50912.2020.9243997>
- [38] Kun, C., Qi, S., Shengkai, L., Chengzhi, P. (2019). Implementation of encoder and decoder for LDPC codes based on FPGA. *Journal of Systems Engineering Electronics*, 30(4): 642-650. <https://doi.org/10.21629/JSEE.2019.04.02>
- [39] Ren, W., Liu, H. (2018) The design and implementation of high-speed codec based on FPGA. In *10th International Conference on Communication Software and Networks (ICCSN)*, Chengdu, China, pp. 427-532. <https://doi.org/10.1109/ICCSN.2018.8488239>
- [40] Boudaoud, A., El Haroussi, M., Abdelmounim, E. (2017). VHDL design and FPGA implementation of LDPC decoder for high data rate. *International Journal of Advanced Computer Science Applications*, 8(4): 257-261. <https://doi.org/10.14569/ijacsa.2017.080435>
- [41] Asif, M., Khan, W.U., Afzal, H.R., Nebhen, J., Ullah, I., Rehman, A.U., Kaabar, M.K. (2021). Reduced-complexity LDPC decoding for next-generation IoT networks. *Wireless Communications Mobile Computing*, 2021: 1-10. <https://doi.org/10.1155/2021/2029560>
- [42] Tsatsaragkos, I., Paliouras, V. (2017). A reconfigurable LDPC decoder optimized for 802.11 n/ac applications. *IEEE Transactions on Very Large Scale Integration Systems*, 26(1): 182-195. <https://doi.org/10.1109/TVLSI.2017.2752086>
- [43] Choi, G., Park, K.B., Chung, K.S. (2018). Optimization of FPGA-based LDPC decoder using high-level synthesis. In *Proceedings of the 4th International Conference on Communication and Information Processing*, pp. 256-259. <https://doi.org/10.1145/3290420.3290441>
- [44] Fajrinada, M.D., Wijayanti, A., Ridwan, M. (2021). Implementation of low-density parity check on field programmable gate array DE1-SoC. In *International Conference on Computer System, Information Technology, and Electrical Engineering (COSITE)*, Banda Aceh, Indonesia, pp. 69-73. <https://doi.org/10.1109/COSITE52651.2021.9649567>
- [45] Liu, Y., Zhang, C., Song, P., Jiang, H. (2017). A high-performance FPGA-based LDPC decoder for solid-state drives. In *IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Boston, MA, USA, pp. 1232-1235. <https://doi.org/10.1109/MWSCAS.2017.8053152>
- [46] Hailes, P., Xu, L., Maunder, R.G., Al-Hashimi, B.M., Hanzo, L. (2018) Hardware-efficient node processing unit architectures for flexible LDPC decoder implementations. *IEEE Transactions on Circuits Systems II: Express Briefs*, 65(12): 1919-1923. <https://doi.org/10.1109/TCSII.2018.2807362>

- [47] Tanner, R. (1981). A recursive approach to low complexity codes. *IEEE Transactions on Information Theory*, 27(5): 533-547. <https://doi.org/10.1109/TIT.1981.1056404>
- [48] Hu, X.Y., Eleftheriou, E., Arnold, D.M. (2005). Regular and irregular progressive edge-growth tanner graphs. *IEEE Transactions on Information Theory*, 51(1): 386-398. <https://doi.org/10.1109/TIT.2004.839541>
- [49] El Hassani, S., Hamon, M.H., Pénard, P. (2010). A comparison study of binary and non-binary LDPC codes decoding. In *SoftCOM 2010, 18th International Conference on Software, Telecommunications and Computer Networks*, Split, Croatia, pp. 355-359.
- [50] Al Ghouwayel, A., Boutillon, E. (2011). A systolic LLR generation architecture for non-binary LDPC decoders. *IEEE Communications Letters*, 15(8): 851-853. <https://doi.org/10.1109/LCOMM.2011.061611.110268>
- [51] Richardson, T.J., Shokrollahi, M.A., Urbanke, R.L. (2001). Design of capacity-approaching irregular low-density parity-check codes. *IEEE Transactions on Information Theory*, 47(2): 619-637. <https://doi.org/10.1109/18.910578>
- [52] Nazar, N., Al-Doori, Q., Alani, O. (2023). Designing a multi-frequency low power Low-Density Parity Check (LDPC) encoder with a Dynamic Voltage and Frequency Scaling (DVFS) Approach. *International Journal of Intelligent Engineering & Systems*, 16(4): 497-511. <https://doi.org/10.22266/ijies2023.0831.40>
- [53] Nazar, N., Al-Doori, Q., Alani, O. (2023). Low Power Low-Density Parity Check Encoder Using Dynamic Voltage and Frequency Scaling Approach. *Mathematical Modelling of Engineering Problems*, 10(1): 14-22. <https://doi.org/10.18280/mmep.100102>
- [54] Venkatesh, D. Y., Mallikarjunaiah, K., Srikantaswamy, M. (2022). A comprehensive review of low density parity check encoder techniques. *Ingénierie des Systemes d'Information*, 27(1): 11-20. <https://doi.org/10.18280/isi.270102>
- [55] Richardson, T.J., Urbanke, R.L. (2001). The capacity of low-density parity-check codes under message-passing decoding. *IEEE Transactions on Information Theory*, 47: 599-618. <https://doi.org/10.1109/18.910577>
- [56] Moreira, J.C., Farrell P.G. (2006). *Essentials of Error-Control Coding*. John Wiley & Sons.
- [57] Zarubica, R., Wilson, S.G., Hall, E. (2007). Multi-Gbps FPGA-based low density parity check (LDPC) decoder design. In *IEEE GLOBECOM 2007-IEEE Global Telecommunications Conference*, Washington, DC, USA, pp. 548-552. <https://doi.org/10.1109/GLOCOM.2007.108>
- [58] Al-Doori, Q., Alani, O. (2015). A multi polynomial CRC circuit for LTE-Advanced communication standard. In *7th Computer Science and Electronic Engineering Conference (CEEC)*, Colchester, UK, pp. 19-23. <https://doi.org/10.1109/CEEC.2015.7332693>
- [59] Chandrasetty, V.A., Aziz, S.M. (2017). *Resource efficient LDPC decoders: From algorithms to hardware architectures*. Academic Press.
- [60] Jose, R., Pe, A. (2015). Analysis of hard decision and soft decision decoding algorithms of LDPC codes in AWGN. In *IEEE International Advance Computing Conference (IACC)*, Bangalore, India, pp. 430-435. <https://doi.org/10.1109/IADCC.2015.7154744>
- [61] Wanjari, A., Kakde, S., Khobragade, A. (2016). Error performance of LDPC decoder using bit flip algorithm. In *International Conference on Communication and Signal Processing (ICCSP)*, Melmaruvathur, India, pp. 0280-0283. <https://doi.org/10.1109/ICCSP.2016.7754139>
- [62] Dhanorkar, P., Kalbande, M. (2017). Design of LDPC decoder using message passing algorithm. In *International Conference on Communication and Signal Processing (ICCSP)*, Chennai, India, pp. 1923-1926. <https://doi.org/10.1109/ICCSP.2017.8286733>
- [63] Zarubica R., Hinton R., Wilson S.G., Hall E.K. (2008) Efficient quantization schemes for LDPC decoders, *MILCOM 2008-2008 IEEE Military Communications Conference*, San Diego, CA, USA, pp. 1-5. <https://doi.org/10.1109/MILCOM.2008.4753231>
- [64] Xu, M., Wu, J., Zhang, M. (2010). A modified offset min-sum decoding algorithm for LDPC codes. In *3rd International Conference on Computer Science and Information Technology*, Chengdu, China, pp. 19-22. <https://doi.org/10.1109/ICCSIT.2010.5564884>
- [65] Wu, X., Song, Y., Jiang, M., Zhao, C. (2010). Adaptive-normalized/offset min-sum algorithm. *Communications Letters*, 14(7): 667-669. <https://doi.org/10.1109/LCOMM.2010.07.100508>
- [66] Kim, S., Sobelman, G.E., Lee, H. (2008). Adaptive quantization in min-sum based irregular LDPC decoder. In *IEEE International Symposium on Circuits and Systems (ISCAS)*, Seattle, WA, pp. 536-539. <https://doi.org/10.1109/ISCAS.2008.4541473>
- [67] Jin, J., Tsui, C.Y. (2009). An energy efficient layered decoding architecture for LDPC decoder. *IEEE Transactions on Very Large Scale Integration Systems*, 18(8): 1185-1195. <https://doi.org/10.1109/TVLSI.2009.2021479>
- [68] Howland, C., Blanksby, A. (2001). Parallel decoding architectures for low density parity check codes. In *IEEE International Symposium on Circuits and Systems (Cat. No. 01CH37196)*, Sydney, NSW, Australia, pp. 742-745. <https://doi.org/10.1109/ISCAS.2001.922344>
- [69] Cocco, M., Dielissen, J., Heijligers, M., Hekstra, A., Huisken, J. (2004). A scalable architecture for LDPC decoding. In *Proceedings Design, Automation and Test in Europe Conference and Exhibition*, Paris, France, pp. 88-93. <https://doi.org/10.1109/DATE.2004.1269212>
- [70] Wang, Z., Jia, Q. (2005). Low complexity, high speed decoder architecture for quasi-cyclic LDPC codes. In *IEEE International Symposium on Circuits and Systems (ISCAS)*, Kobe, Japan, pp. 5786-5789. <https://doi.org/10.1109/ISCAS.2005.1465953>
- [71] Jiang, N., Peng, K., Yang, Z. (2008). Flexible low-complexity decoding architecture for QC-LDPC codes. In *11th IEEE Singapore International Conference on Communication Systems*, Guangzhou, China, pp. 1316-1320. <https://doi.org/10.1109/ICCS.2008.4737396>
- [72] Chen, J., Dholakia, A., Eleftheriou, E., Fossorier, M.P., Hu, X.Y. (2005). Reduced-complexity decoding of LDPC codes. *IEEE Transactions on Communications*, 53(8): 1288-1299. <https://doi.org/10.1109/TCOMM.2005.852852>
- [73] Hameed, S.M., Abdulsatar, S.M., Sabri, A.A. (2021). Performance enhancement for visible light communication based ADO-OFDM. *Optical Quantum Electronics*, 53(6): 339. <https://doi.org/10.1007/s11082-021-02965-1>

- [74] Hashim, A.T., Hasan, A.M., Abbas, H.M. (2020). Design and implementation of proposed 320 bit RC6-cascaded encryption/decryption cores on altera FPGA. *International Journal of Electrical and Computer Engineering (IJECE)*, 10(6): 6370-6379. <https://doi.org/10.11591/ijece.v10i6.pp6370-6379>
- [75] Al-Tahar, I.A., Al-Shueli, A. (2023). An enhanced frequency estimation algorithm using a three-point spectral interpolation method. *Ingenierie des Systemes d'Information*, 28(3): 761-766. <https://doi.org/10.18280/isi.280327>
- [76] Hasan, A.F., Al-Doori, Q.F. (2021). Dynamic power consumption in CMOS N bit full-adder circuit. *Engineering Technology Journal*, 39(5): 754-767. <https://doi.org/10.30684/etj.v39i5A.1846>
- [77] Ali, I.H. (2017). Implement wireless transceiver system based on convolutional coding; aided by soft-bit decoding. *Iraqi Journal of Computers, Communications, Control & Systems Engineering (IJCCCE)*, 18(1): 49-55. <https://doi.org/10.33103/uot.ijece.18.1.5>
- [78] Abdulsatar, S.M., Saleh, M.A., Abass, A., Ali, M., Yaseen, M.A. (2021). Bidirectional hybrid optical communication system based on wavelength division multiplexing for outdoor applications. *Optical Quantum Electronics*, 53: 1-11. <https://doi.org/10.1007/s11082-021-03252-9>
- [79] Ahmad, I.A., Al-Nayar, M.M.J., Mahmood, A.M. (2023). Dynamic Low Power Clustering Strategy in MWSN. *Mathematical Modelling of Engineering Problems*, 10(4): 1249-1256. <https://doi.org/10.18280/mmep.100417>
- [80] Pignoly, V., Le Gal, B., Jego, C., Gadat, B. (2018). High data rate and flexible hardware QC-LDPC decoder for satellite optical communications. In *IEEE 10th International Symposium on Turbo Codes and Iterative Information Processing (ISTC)*, Hong Kong, China, pp. 1-5. <https://doi.org/10.1109/ISTC.2018.8625274>
- [81] Nikishkin, P., Goriushkin, R., Vinogradov, N., Likhobabin, E., Vityazev, V. (2022). High throughput FPGA implementation of min-sum LDPC decoder architecture for wireless communication standards. In *24th International Conference on Digital Signal Processing and its Applications (DSPA)*, Moscow, Russian Federation, pp. 1-5. <https://doi.org/10.1109/DSPA53304.2022.9790744>
- [82] Masera, G., Quaglio, F., Vacca, F. (2007). Implementation of a flexible LDPC decoder. *IEEE Transactions on Circuits*, 54(6): 542-546. <https://doi.org/10.1109/TCSII.2007.894409>