A Novel Switched Capacitor Boost Derived Multilevel Hybrid Converter Modeling and Analysis

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1. INTRODUCTION

The solar photovoltaic system is a promising and predominant system among all the renewable energy sources [1]. The low output voltage provided by the SPV system has to be boosted and inverted for dc and ac applications respectively [2]. The output of a single voltage source inverter is not adequate for medium and high power applications as it depends on the amplitude of the input source voltage. For such applications, VSI is cascaded as a multilevel inverter [3] and solar photovoltaic-based cascaded multilevel inverter is a serious research in the recent days. Compared to neural point clamped MLI and flying capacitor MLI, the cascaded configuration uses lesser number of devices for an increase in number of levels [4-5]. Nowadays researchers mainly focus on the design of reduced switch cascaded MLI [6] and hybrid MLI [7] topologies to extract the higher number of output voltage levels. Boost derived multilevel hybrid converter is one of the hybrid MLI proposed in [8] which produces multilevel ac output along with dc output. It is formed by cascading two or more BDHC [9]. A switched capacitor (SC) cell is connected in front of the BDHC is called as SCBDHC. For achieving higher ac gain in the multilevel configuration, SCBDHC units are connected serially and the configuration is referred as switched capacitor boost derived multilevel hybrid converter (SCBDMHC).

The SCBDMHC is a triple output and single input converter, which produces multilevel ac output and two boosted dc outputs simultaneously. This paper explains the proposed circuit configuration, its modes of operation, dynamic model and the closed loop control scheme. The robustness of the SCBDMHC is verified with load, line and reference variation.

This paper is structured into seven sections. Section 2 describes the circuit operation while Section 3 focuses on switching strategy. Section 4 explains the dynamic model of the converter and Section 5 presents closed loop PI controller design. The simulated results are explained in Section 6. Section 7 provides a fair summing of all the Sections.

2. PROPOSED CONVERTER - SCBDMHC

2.1 Circuit configuration

Figure 1. Proposed SCBDMHC circuit

In the configuration of the proposed converter depicted in Figure 1, two SCBDHC units are connected in series to produce the five level ac output and separate dc outputs simultaneously. The switched capacitor cell has two switches $S_{11}$ and $S_{12}$, a capacitor $C_{s1}$, a diode $D_{s1}$ and a source resistor $R_{s1}$ for first level circuit. The input sources $V_{idc1}$ and $V_{idc2}$, bridge network switches $Q_{11}$ to $Q_{14}$, $Q_{21}$ to $Q_{24}$ and SC cell switches $S_{11}$, $S_{12}$, $S_{21}$, and $S_{22}$ are operated for both ac and dc operations. In the conventional multilevel inverter, the output
phase voltage is the sum of the input voltages where as in the proposed SCBDMHC, as the input voltages are boosted by the switched capacitor cell which present in the input side, the output phase voltage is the boosted sum of the input voltages. Besides, each bridge along with the switched capacitor circuit produces separate boosted dc output along with the multilevel ac output.

2.2 Modes of operation

The circuit is operated with two modes: boosting mode and inverting mode.

2.2.1 Boosting mode

Boosting mode is a high frequency switching mode, which is further divided into shoot-through interval mode \((0 < t < \delta T)\) and power interval mode \((\delta T < t < (1-\delta) T)\) where \(\delta\) is the duty ratio. When the same leg of switches \(Q_{11}, Q_{14}\) and the SC cell switch \(S_{12}\) are ON as shown in the Figure 2, the converter operates in shoot-through interval mode and when the switches \(Q_{11}, Q_{12}\) and \(S_{11}\) are ON as shown in the Figure 3, the converter operates in power interval mode. During shoot-through interval, the capacitors \(C_{14}\) and \(C_{22}\) get charged and the inductors \(L_1\) and \(L_2\) store energy from the source. The diode \(D_1\) and \(D_2\) get reverse biased. Hence no current flows from source to dc load as well as ac load. During the power interval mode, the source current is divided and flowing through the dc and ac loads.

![Figure 2. Shoot-through interval mode of SCBDMHC](image)

2.2.2 Inverting mode

The inverting mode is a low frequency switching mode. This mode is further divided into level 1 and level 2 intervals. During level 1 interval, the switches \(Q_{11}, Q_{12}\) and \(Q_{21}\) conduct and the first input source \(V_{idc1}\) connects with the ac load, which provides three level output across \(R_{ac}\). During level 2 interval, the switches \(Q_{11}, Q_{12}, Q_{21}\) and \(Q_{22}\) conduct and the input sources \(V_{idc1}\) and \(V_{idc2}\) connect with the ac load, which provides five level output across \(R_{ac}\). Each phase level internally consists of boosting operation.

![Figure 3. Power interval mode of SCBDMHC](image)

2.3 Output voltages of SCBDMHC

In SCBDMHC, identical elements in each cell are assumed to have same values, for e.g. \(L_1 = L_2\), \(R_{dc1} = R_{dc2}\) etc. The number of voltage levels \((m)\) in the phase voltage of SCBDMHC is \(m=(2N+1)\), where \(N\) is the number of SCBDHC units. The SCBDMHC dc output voltage of each cell is given in the equation (1):

\[
v_{odc1}(t) = \frac{(2-\delta)V_{idc1}(t)}{1-\delta}; \quad v_{odc2}(t) = \frac{(2-\delta)V_{idc2}(t)}{1-\delta}
\]

(1)

The five level SCBDMHC ac peak output voltage is given in the equation (2):

\[
v_{oac}(t) = \frac{(2-\delta)V_{idc1}(t)}{1-\delta} + \frac{(2-\delta)V_{idc2}(t)}{1-\delta}
\]

(2)

In general, it is expressed as:

\[
v_{oac}(t) = \sum_{m=1}^{N} \frac{(2-\delta)V_{idc}(t)}{1-\delta} = \sum_{m=1}^{N} V_{odc}(t)
\]

(3)

From the equations (1) to (3), it is understood that the dc and ac outputs of SCBDMHC is controlled by the duty cycle \(\delta\) and the ac peak voltage depends on the dc output voltage.

3. SWITCHING STRATEGY

The switching sequence adopted for the SCBDMHC is tabulated in the Table 1. The reference voltage is a sinusoidal waveform with the frequency \(f_0\) and the amplitude \(m_a\), called modulation index. For SCBDMHC the \(m_a\) has the range of \(0 < m_a < 0.5\). The output phase voltage has its fundamental component \(v_f(t)\) at \(f_0\) and can be expressed as in (4):

\[
v_f(t) = m_a N V_{idc} \sin(2\pi f_0 t)
\]

(4)
This reference signal is compared with the two dc constants \( V_{a1}, V_{a2} \) as shown in the Figure 4 to control the level of the SCBDMHC. A triangular carrier pulse \( V_{ct} \) is compared with a dc signal \( V_{d} \) as shown in Figure 5, which controls the boosting period of SCBDMHC. The signals so generated separately for inverter operation and boost operation are logically added as shown in the Figure 6, and the appropriate gate pulses \( G_{11} \) to \( G_{24} \) and \( G_{25} \) to \( G_{28} \) are produced.

4. DYNAMIC MODEL OF SCBDMHC

4.1 Mathematical modeling of the SCBDMHC

4.1.1 Level1 equations

The dynamic model of the SCBDMHC is derived to develop the transfer function of the system. Level 1 represents the first source that is connected with the ac load by operating the corresponding switches as given in the Table 1. The shoot-through interval mode and power interval mode dynamic equations are derived by applying the KVL and KCL, and are described in (5) to (8).

During shoot-through interval \((0 < t < \delta T)\)

\[
\begin{align*}
C_{s1} \frac{dv_{ca1}(t)}{dt} &= \frac{V_{idc1}(t)}{R_{s1}} - \frac{v_{ca1}(t)}{R_{s1}} - i_{ca1}(t), \\
C_{s2} \frac{dv_{ca2}(t)}{dt} &= \frac{V_{idc2}(t)}{R_{s2}} - \frac{v_{ca2}(t)}{R_{s2}} - i_{ca2}(t), \\
L_{1} \frac{dL_1(t)}{dt} &= v_{ca1}(t), \\
L_{2} \frac{dL_2(t)}{dt} &= v_{ca2}(t), \\
C_{1} \frac{dv_{odc1}(t)}{dt} &= -\frac{v_{idc1}(t)}{R_{dc1}}, \\
C_{2} \frac{dv_{odc2}(t)}{dt} &= -\frac{v_{idc2}(t)}{R_{dc2}} \\
\end{align*}
\]

Table 1. Switching sequence of SCBDMHC

<table>
<thead>
<tr>
<th>Switching sequences</th>
<th>AC Output Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 ( Q_{11} ) 0 ( Q_{12} ) 0 ( Q_{13} ) 0 ( Q_{14} ) 0 ( Q_{21} ) 0 ( Q_{22} ) 0 ( Q_{23} ) 0 ( Q_{24} )</td>
<td>( V_{dc} ) 0V</td>
</tr>
<tr>
<td>Positive Hall 1 1 1 0 1 1 0 ( B )</td>
<td>( (2 - \delta)V_{idc1} )</td>
</tr>
<tr>
<td>Negative Hall 0 0 0 1 0 0 0 ( B )</td>
<td>(-V_{idc1} )</td>
</tr>
</tbody>
</table>

\( B \)- high frequency boosting condition, 1-ON condition, 0-OFF condition.

Figure 4. Generation of pulses for inverting operation of SCBDMHC

Figure 5. Generation of pulses for boosting operation of SCBDMHC

Figure 6. Logic diagram for gate pulses of SCBDMHC

During power interval \((\delta T < t < (1 - \delta)T)\)

\[
\begin{align*}
C_{s1} \frac{dv_{ca1}(t)}{dt} &= i_{ca1}(t), \\
C_{s2} \frac{dv_{ca2}(t)}{dt} &= i_{ca2}(t), \\
L_{1} \frac{dL_1(t)}{dt} &= V_{idc1}(t) + v_{cx}(t) - v_{odc1}(t), \\
L_{2} \frac{dL_2(t)}{dt} &= V_{idc2}(t) + v_{cx}(t) - v_{odc2}(t), \\
C_{1} \frac{dv_{odc1}(t)}{dt} &= i_{L1}(t) - i_{ac}(t) - \frac{V_{odc1}(t)}{R_{dc1}}, \\
C_{2} \frac{dv_{odc2}(t)}{dt} &= i_{L2}(t) - i_{ac}(t) - \frac{V_{odc2}(t)}{R_{dc2}} &
\end{align*}
\]
where \(i_{11}, i_{12}\) are the input current through the inductor \(L_1\) and \(L_2\) respectively. The inverter side equation is given in (7):

\[
L_1\frac{di_{ac}(t)}{dt} = V_{idc1}(t) + v_{cs1}(t) - R_{ac}i_{ac}(t)
\]

### 4.2 State-space representation

The system descriptive equations (5) to (8) are rearranged in the form of state equations. The level 1 averaged state equation is given in (9). Similarly the level 2 state and output equations are given in (10) and (11) respectively. In general, the level \(n\) state and output equations for SCBDMHC are given in the equations (12) and (13) respectively.
Linearizing (5) to (8) by adding the small perturbation in the input, output and state variables, around the equilibrium point and separating the dynamic ac small signal terms from the dc steady state component as in [10], the following dynamic model (14) is obtained:

\[ \dot{x}(t) = Ax(t) + Bu(t) + E\delta(t) \]  

where the state matrix A and the input matrix B are given in (10). E matrix corresponding to \( \delta(t) \), \( \hat{x}(t) \) and \( \hat{u}(t) \) are given in (15):

\[
E = \begin{pmatrix}
\frac{V_{Vdc1}-V_{cst1}}{V_{Vdc2}-V_{cst2}} - \frac{2L_{11}}{C_{st1}} & \frac{2L_{12}}{C_{st2}} & -\frac{V_{Vdc1}}{V_{Vdc2}} - \frac{L_{11}}{L_{2}} & -\frac{L_{12}}{L_{2}} - \frac{i_{ac}}{L_{1}} \\
\frac{V_{Vdc1}-V_{cst1}}{V_{Vdc2}-V_{cst2}} - \frac{2L_{11}}{C_{st1}} & \frac{2L_{12}}{C_{st2}} & -\frac{V_{Vdc1}}{V_{Vdc2}} - \frac{L_{11}}{L_{2}} & -\frac{L_{12}}{L_{2}} - \frac{i_{ac}}{L_{1}} \\
\end{pmatrix}
\]

\[
\dot{x}(t) = \begin{pmatrix}
\frac{\delta_{Vdc1}}{R_{ac}L_{ac}} \\
\frac{\delta_{Vdc2}}{R_{ac}L_{ac}} \\
\end{pmatrix}
\]

\[
\hat{u}(t) = \begin{pmatrix}
\hat{V}_{idc1} \\
\hat{V}_{idc2} \\
\end{pmatrix}
\]

4.3 Numerical validation

The parameters considered for the simulation of SCBDMHC are specified in Table 2. These values are substituted in the equation (10) and the resultant state and input matrices obtained are given in equation (16).

**Table 2. Parameters of SCBDMHC**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage (( V_{Vdc1} ) and ( V_{Vdc2} ))</td>
<td>40V</td>
</tr>
<tr>
<td>Input Inductor (( L_{1} ) and ( L_{2} ))</td>
<td>5mH</td>
</tr>
<tr>
<td>DC Capacitor (( C_{1} ) and ( C_{2} ))</td>
<td>1mF</td>
</tr>
<tr>
<td>DC load resistor (( R_{dc1} ) and ( R_{dc2} ))</td>
<td>20Ω</td>
</tr>
<tr>
<td>AC load resistor (( R_{ac} ))</td>
<td>50Ω</td>
</tr>
<tr>
<td>Switching frequency (f)</td>
<td>10KHz</td>
</tr>
<tr>
<td>Switched capacitor (( C_{31} ) and ( C_{32} ))</td>
<td>1mF</td>
</tr>
<tr>
<td>Source Resistor (( R_{31} ) and ( R_{32} ))</td>
<td>0.01 Ω</td>
</tr>
</tbody>
</table>

\[
A = \begin{pmatrix}
-51000 & 0 & -20 & 0 & 0 & 0 \\
0 & -51000 & 0 & -20 & 0 & 0 \\
200 & 0 & 0 & 0 & -98 & 0 \\
0 & 200 & 0 & 0 & 0 & -98 \\
0 & 0 & 490 & 0 & -50 & 0 \\
0 & 0 & 0 & 490 & 0 & -50 \\
49 & 0 & 0 & 0 & 0 & -2450 \\
\end{pmatrix}
\]

\[
B = \begin{pmatrix}
40 \\
51000 \\
98 \\
98 \\
98 \\
98 \\
98 \\
\end{pmatrix}
\]

\[
C = (1 \ 1 \ 0 \ 0 \ 1 \ 1 \ 0), \ D = (0) \]

To solve the state equations, m-file programming in MATLAB is used and the state values obtained is given in equation (17):

\[
x(t) = \begin{pmatrix}
V_{Vdc1}(t) \\
V_{Vdc2}(t) \\
i_{L2}(t) \\
i_{L2}(t) \\
V_{odc1}(t) \\
V_{odc2}(t) \\
i_{ac}(t)
\end{pmatrix}
\]
\( x(t) = (39.9936V \quad 39.9936V \quad 16.41A \quad 16.41A \quad 121.6195V \quad 121.6195V \quad 3.9A)^T \) \quad (17)

In order to validate the developed model of the system, the circuit is simulated using MATLAB/Simulink with the same parameters specified in Table 2. Input voltage is set to 40V with the duty ratio of 0.51 and modulation index of 0.49. The simulated output voltage across the loads and current through the loads observed are depicted in the Figure 7 and Figure 8 respectively. These results are tabulated in the Table 3 and compared with the values obtained from the mathematical model.

![Figure 7. Open loop input and output voltage waveforms](image)

![Figure 8. Open loop input and output current waveforms](image)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output dc voltage ((V_{dc1} to V_{dc2}))</td>
<td>Theoretical: 121V</td>
</tr>
<tr>
<td>Output ac voltage ((v_{ac}))</td>
<td>195V</td>
</tr>
<tr>
<td>Input Current ((i_{L1} to i_{L2}))</td>
<td>16.4A</td>
</tr>
<tr>
<td>Output dc current ((i_{dc1} to i_{dc2}))</td>
<td>6.08 A</td>
</tr>
<tr>
<td>Output ac current ((i_{ac}))</td>
<td>3.9A</td>
</tr>
</tbody>
</table>

From the Figure 7 the output dc voltage is found to be 121.62 V and the ac voltage is 179 V. Similarly from Figure 8 the input current is noted as 17.4 A, the dc output current is 6 A and ac output current is 3.54 A.

The proposed SCBDMHC output voltage is compared with the conventional MLI. When 40 V dc is supplied as input for the five level multilevel inverter, it produces the ac peak output of 80 V, whereas the five level SCBDMHC, produced the ac output peak voltage of 243 V. This will be \( \frac{243}{80} \) times higher than the conventional MLI output.

4.4 Transfer function

Using the equations (14) and the Table 2 the dc output voltage to control transfer function (18) is developed.

\[
\frac{V_{odc}(s)}{\delta(s)} = \frac{-1.25 \times 10^4 s^6 - 1.3 \times 10^5 s^5 - 3.8 \times 10^6 s^4 - 1.48 \times 10^7 s^3 + 4.15 \times 10^8 s^2 + 4.5 \times 10^9 s^1 + 9.49 \times 10^{10} + 6.66 \times 10^{12} + 9.197 \times 10^{14} s^2 + 6.42 \times 10^{17} s^3 + 3.727 \times 10^{19} s^4 + 1.47 \times 10^{22} s^5}{s^6 + 3 \times 10^{10} s^5 + 2 \times 10^{12} s^4 + 1.2 \times 10^{14} s^3 + 6.195 \times 10^{15} s^2 + 1.953 \times 10^{17} s^1 + 4.1 \times 10^{19}}
\]

5. CLOSED LOOP SCHEME OF SCBDMHC

Figure 9 shows the closed loop control scheme of the switched capacitor boost derived multilevel hybrid converter. A part of dc output voltage is fed back from the SCBDMHC and compared with the set point value, and the error occurred is processed by the PI controller [11] whose parameters are tuned using Zeigler Nichols oscillation method. The controller parameters \( K_p=0.0072 \) and \( K_i=5.01 \) are obtained. The simulation results with the closed loop circuit is discussed in the next section.

![Figure 9. Closed loop scheme of SCBDMHC](image)

6. SIMULATION RESULTS AND ANALYSIS

The closed loop system of the SCBDMHC is tested with line regulation, load regulation and reference variation.

6.1 Line regulation of SCBDMHC

To verify the performance of the controller under supply variations, the load resistance is kept at a fixed value of \( R_{dc}=20 \Omega \) and \( R_{ac}=50 \Omega \), variation is incorporated only in the supply side. The reference voltage across the dc load is set as 150 V. The supply voltage is maintained at 45V until \( t=0.75s \) and a step change is given to vary the input voltage to 35 V. The corresponding dc output voltage is regulated to 150 V as depicted in Figure 10. The ac output voltage is also regulated for 230 V as shown in the Figure 6c.

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6.2 Load regulation of SCBDMHC

The input voltage is set as 40 V and the reference dc output voltage is at 150 V and ac output voltage is at 230 V. Under this condition, the dc load is varied from 5 Ω to 25 Ω at 0.75 sec as shown in the Figure 11(a).

The sudden rise in the load resistance, results in a corresponding peak overshoot to 250V in the output voltage, which gives a significant variation from the desired set value of 150 V. The controller responds instantaneously and adjusts the duty ratio in order to generate an output voltage to the desired set reference value, within a settling time of \( t_s = 0.25 \) sec as depicted in Figure 11(b). To support this result, the corresponding variation in the load current has also been presented in Figure 11(c) and it decreases from 30 A to 6 A.

Similarly, ac load resistance \( R_{ac} \) is varied from 40 Ω to 80 Ω at the time \( t = 0.75 \) sec. For a sudden increase in load, the controller responds effectively and it is observed that the output voltage is maintained constant, irrespective of the change in load providing load regulation as shown in Figure 12(b). The corresponding variation in the load current is presented in Figure 12(c) and it is reduced from 5.75 A to 2.8 A.

6.3 Reference variation of SCBDMHC

Here both the input supply voltage and load resistance are maintained constant and the controller performance is verified by varying the reference value. DC input voltage is fixed at 40 V and load resistance values are maintained at \( R_{dc} = 20 \) Ω and \( R_{ac} = 50 \) Ω. For dc side, initially, the reference voltage is set at 200V and the reference value is changed to 150 V at \( t = 0.75 \) sec. Similarly the ac output voltage reference varies from 282.9 V to 212.1 V rms at \( t = 0.75 \) sec. The dc and ac output voltage waveforms depicted in Figure 13, reveal the controller performance in tracking the respective set reference values.

7. CONCLUSION

In this paper, a novel switched capacitor boost derived multilevel hybrid converter is proposed which is capable of supplying boosted dc and multilevel ac output simultaneously for SPV application. The state-space modeling equations are derived and validated with the simulated results. A closed loop scheme for the SCBDMHC has been developed and to prove its robustness the system performance is tested with line regulation, load regulation and reference variation. From the results, it is concluded that the SCBDMHC has the higher ac gain which is \( \frac{1-\delta}{1-\delta} \) times more than the conventional MLI.
REFERENCES


NOMENCLATURE

\( V_{idc1}, V_{idc2} \) Input sources
\( v(t) \) A dc signal
\( V_1, V_2 \) dc reference signals for level triggering
\( L_1, L_2 \) Inductors \( H \)
\( m \) Number of input phase voltage
\( m_a \) Modulation index
\( \chi \) State vector matrix
\( V_{odc} \) Output voltage of the DC load
\( V_{oac} \) Output voltage of the AC load
\( Q_{11} \) to \( Q_{14} \) Bridge network switches for I stage
\( Q_{21} \) to \( Q_{24} \) Bridge network switches for II stage
\( R_{ac} \) AC load resistor
\( R_{dc} \) DC load resistor
\( s \) Laplace Transform factor
\( T \) Simulation time period
\( V_{odc1}, V_{odc3} \) Voltage across capacitors \( C_1 \) to \( C_3 \)
\( \hat{v}(t) \) Small signal AC variations for \( V(t) \)

Greek symbol

\( \delta \) Duty ratio

Subscripts

odc Output dc
oac Output ac