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NOMENCLATURE

V_{idc1}, V_{idc2}	Input sources
v(t)	A dc signal
V_1, V_2	dc reference signals for level triggering V
L_1, L_2	Inductors H
m	Number of input phase voltage
m_a	Modulation index
x	State vector matrix
V_{odc}	Output voltage of the DC load V
V_{oac}	Output voltage of the AC load V
Q_{11} to Q_{14}	Bridge network switches for I stage
Q_{21} to Q_{24}	Bridge network switches for II stage
R_{ac}	AC load resistor
R_{dc}	DC load resistor
s	Laplace Transform factor
T	Simulation time period
V_{odc1}, V_{odc3}	Voltage across capacitors C_1 to C_3
$\hat{v}(t)$	Small signal AC variations for V(t)

Greek symbol

δ	Duty ratio

Subscripts

odc	Output dc
oac	Output ac