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Design of Control System Using Online Tuning of PI Controllers for Three-Phase Active Front End Neutral Point Clamped Three-Level Converter

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ABSTRACT

In conventional DC link AC-AC converter system, uncontrolled front end converter has inherent problem of power quality. To overcome the problem associated with uncontrolled front end converter, multilevel front end converter will be good choice for high power applications. In the paper, unity power factor control system (UPC) for active front end (AFE) neutral point clamped (NPC) 3-level converter is presented. PI controllers are used in UPC and for tuning of PI controllers it is essentially required to know the different time constants with their gains exactly for evaluating the optimized controller parameters for steady operation of the NPC rectifier. In this paper a simplified and accurate method of online tuning of PI controllers in UPC is derived and implemented for three phase AFE NPC 3-level converter. Complete design procedure for the design of control system for AFE NPC 3-level is also presented in this paper. Based on developed model, simulations are carried in MATLAB/SIMULIK environment. Experimentation results confirm the simulation results.

1. INTRODUCTION

Active front end converters have been widely used in variable speed drives [1]. Uncontrolled device or SCRs based converters draws currents rich in harmonics and reactive component of the current from the source creates the issue of power quality [2, 3]. High power factor converters became the inherent part of AC-DC conversion [4-8] an effectively used to overcome these issues and for improved power quality. But these high-power factor converters utilize high voltage rating devices and they are having issues of high voltage stress across the device, dv/dt, high common mode voltage, high switching frequency etc. [9-12]. The performance of multilevel converter is excellent in terms of improved power quality, less ripple in output voltage, less voltage stress and low electromagnetic interference with neighbouring communication lines as compared to high power factor converters [13-26]. Amongst the conventional topologies of multilevel structure, Diode-clamped multilevel converter is used for power conditioning now a days [9-11].

A simplified current controlled controller is designed and developed for controlling output voltage and for maintaining the power factor at unity. The controller is comprising of PI controllers and tuning of PI controllers which is easy to implement in real time application is still brain storming research for researchers. For tuning of PI controllers there so many well-known optimisation techniques like Artificial Neural Network, Genetic Algorithm, Particle Sworn Optimization etc. are available for getting optimised controller parameters [27, 28]. These optimising techniques have their own advantages and disadvantages and provide solution based on available mathematical model of the system. Another aspect which ensures the accuracy of the solution provided by these techniques is the constraints defined for getting desired output.

Tuning of converters requires the optimization of controller parameters for defined constraints and stable operation of the system. Therefore, an appropriate optimization technique is required to use for the tuning of controllers as almost, all are doing. The available technique till now is system dependent and has their own advantages and disadvantages [29-31]. Also, there is serious issue of real time implementation with evaluated tuned parameters of the controller.

In the present scenario, almost all simulations are carried out in the MATLAB/SIMULINK environment because the same Simulink model can be used with sophisticated controller like dSPACE 1104,1103, microLabbox etc. as well as with low cost controllers like STM32 microcontroller for real time implementation.

Therefore, there is an attempt to use available optimization software with MATLAB/SIMULINK environment to tune the controllers for the design and development of complex system. In this paper the author designed a complex 3-phase AFE NPC 3-level converter with controller using optimization software available in Simulink Design Optimization library. The proposed system is also developed in the laboratory and confirms that it is easier way to tune the controllers with more accuracy. The term online is used because tuning technique used is a part of MATLAB/SIMULINK environment and it optimised the controller parameters by communicating the Simulink model internally. This will defiantly save the time as well as digital space requirement and improve the performance of the system.

The whole paper is organised in seven (07) sections. In section 2, survey of literatures related to the tuning of controllers is carried out for establishing the appropriate research gap. There is description about the 3-phase AFE NPC 3-level converter in section 3. The complete design of

controller is presented in section 4. Section 5 deals with the simulation results of proposed tuning technique for the controller of 3-phase AFE NPC 3 level converter. The hardware results for the validation of simulation results of the proposed system are presented in section 6 followed by conclusion in section 7.

2. TUNING OF CONTROLLERS: A SURVEY

There are many tuning methods are proposed till now to tune the controller for considerable improvements in performance of controller. The merits and de-merits of some commonly used tuning method are discussed in Table 1.

There are literatures related to the tuning methods of PI controllers [27-31]. The objective all are same to assess the relative control effort and robustness of these PI controllers when tuned for the same level of performance. Some methods with simple formulas use little information of process dynamics to obtain moderate performance, however it often need to retune by trial and error depend on those results. More sophisticated tuning method can get rise to considerable improvements in performance, but they are also more demanding computationally and depend on more information of process dynamics.

The above analysis clearly shows that the performance of the controller depends on the optimization of the parameters. The choice of method should be based on the characteristics of the process and performance requirements. Therefore, author attempted to use optimization software available with MATLAB/SIMULINK library to tune the PI controllers to maintain the balance between characteristics of the process and performance requirement. The feature of online tuning method using signal constraint is that its compliance most of requirement for tuning of controller without much sacrificing the performance of the controller. This is because it is inbuilt optimization software in MATLAB/SIMULINK and in most of the sophisticated controller like dSPACE 1104, 1103, microlabbox etc., Simulink model can effectively build and run. Therefore, the communication of the Simulink model with the inbuilt optimization software is very fast. Also, it minimizes the complexity of the controller which is important from the practical implementation point of view.

2.1 Tuning of PI controllers using Signal Constraint block

In this section the technical aspect of the tuning of controller using optimization software available in MATLAB/SIMULINK library has been explained. For the tuning of a controller following parameters of the signal has to be taken into the consideration.

1) Rise time
2) Maximum overshoot
3) Settling time
4) Steady state error.

When optimization of parameters of a Simulink model to meet time-domain design requirements attempted, Simulink Design Optimization software automatically converts the requirements into a constrained optimization problem and then solves the problem using optimization techniques. The constrained optimization problem iteratively simulates the Simulink model, compares the results of the simulations with the constraint objectives, and uses optimization methods to adjust tuned parameters to better meet the objectives.

Table 1. Comparison of different methods for tuning the controllers

Method	Key Features	Disadvantages
Ziegler-Nichols (Z-N) method	It is most commonly used method for tuning and has very strong impact on controller. The tuning methods are based on a step response experiment and on a frequency response experiment.	The main drawback of the method is the use of information for characterization of process dynamics with poor damping and poor robustness.
Haalman and λ - Tuning method	In this method the process poles and zeros are canceled by poles and zeros in the controller. With this feature a specified closed-loop transfer function can be obtained that gives the desired performance which the key feature of the controller.	But the issue with the cancellation is the chance of uncontrollable modes in the closed-loop system and the response to load disturbances may be poor when the canceled poles are slow in comparison with the dominant poles
Pole placement method	This method is preferably used for low order system like first or second order system.	For higher order system the controller becomes complex.
Graphic tuning method	This is the graphical method and most intuitive design method. The tuning method is based on finding the centroids of stability regions in the controller parameter space, considering a point which is situated away from the boundaries of the stability region, and consequently the controller, which is tuned based on such a point, will be nonfragile.	The main disadvantage of this method is it is very time-consuming and neglect of the other important performance indicators.
M -constrained integral gain optimization (MIGO)	It is non-convex optimization method to obtain the controller parameters This optimization can be solved by some iterative algorithm such as Newton-Raphson or Genetic algorithms.	The issue with this method is that it requires considerable amount of computational capacity.
AMIGO and Kappa-Tau tuning method	AMIGO is an approximation of MIGO and can be used for wide range of system. Processes with lag dominated dynamics, balanced lag and delay or dominated dynamics can use this method to tuning controller to get an acceptable performance. Kappa-Tau tuning method is very similar to the MIGO method. The different is only the Kappa-Tau tuning method is an approximation to pole placement.	The performance of the controller using this method is inferior as compared to MIGO
Internal model principle (IMC) method	The key feature of this method is that it has only one user-defined tuning parameter, which attracts many industrial users.	The excellent set-point response can be obtained by the IMC, but the response to load disturbances is often poor.

The software first formulates the problem for parameter optimization. For each optimization algorithm, the software formulates one of the following types of minimization problems

1) Feasibility
2) Tracking
3) Mixed Feasibility and Tracking.

➢ **Feasibility Problem and Constraint Formulation**

Feasibility means that the optimization algorithm finds parameter values that satisfy all constraints to within specified tolerances but does not minimize any objective or cost function in doing so. In the following Figure 1, x_1, x_3, and x_n represent a combination of parameter values P_1 and P_2 and are feasible solutions because they do not violate the lower bound constraint.

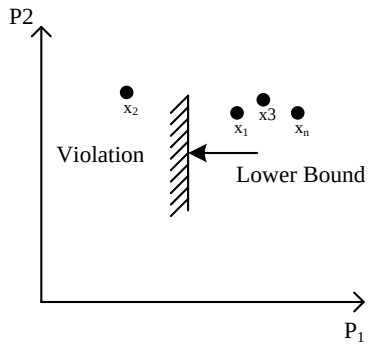


Figure 1. Feasibility response

In a Simulink model, one can constrain a signal by specifying lower and upper bounds in a Signal Constraint block, as shown in the following Figure 2.

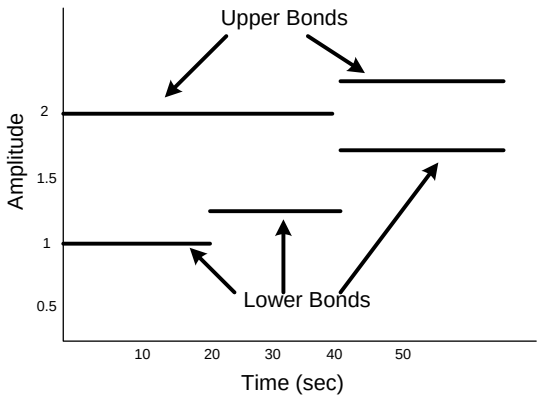


Figure 2. Appling the constraints on signal using Signal Constraint block

These constraints are *piecewise linear bounds*. A piecewise linear bound y_{bnd} with n edges can be represented as:

$$y_{bnd}(t)=\begin{cases} y_1(t) & t_1 \le t \le t_2 \\ y_2(t) & t_2 \le t \le t_3 \\ \vdots & \vdots \\ y_n(t) & t_n \le t \le t_{n+1} \end{cases} \quad (1)$$

The software computes the signed distance between the simulated response and the edge. The signed distance for lower bounds is:

$$c=\begin{bmatrix} \max\limits_{t_1 \le t \le t_2} & y_{bnd}-y_{\sin} \\ \max\limits_{t_2 \le t \le t_3} & y_{bnd}-y_{\sin} \\ \max\limits_{t_n \le t \le t_{n+1}} & y_{bnd}-y_{\sin} \end{bmatrix} \quad (2)$$

where, y_{sim} is the simulated response and is a function of the parameters being optimized.

The signed distance for upper bounds is:

$$c=\begin{bmatrix} \max\limits_{t_1 \le t \le t_2} & y_{\sin}-y_{bnd} \\ \max\limits_{t_2 \le t \le t_3} & y_{\sin}-y_{bnd} \\ \max\limits_{t_n \le t \le t_{n+1}} & y_{\sin}-y_{bnd} \end{bmatrix} \quad (3)$$

If *all* the constraints are met ($c \le 0$) for some combination of parameter values, then that solution is said to be feasible. In the following Figure 3, x_1 and x_3 are feasible solutions.

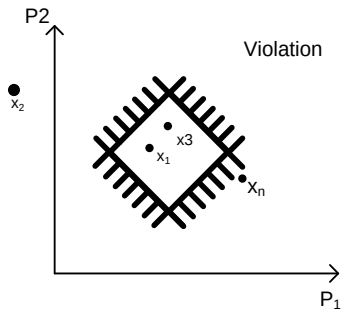


Figure 3. Possible feasible solutions using Signal Constraint block

When the model has multiple Signal Constraint blocks or vector signals feeding a Signal Constraint block, the constraint vector is extended with the constraint violations for each signal and bound:

$$C=[c_1;c_2;\cdots;c_n] \quad (4)$$

➢ **Tracking Problem**

In addition to lower and upper bounds, you can specify a reference signal in a Signal Constraint block, which the Simulink model's output can track. The tracking objective is a sum-squared-error tracking objective.

The reference signal can be specified as a sequence of time-amplitude pairs:

$$y_{ref}(t_{ref}), t_{ref} \in \{T_{ref0}, T_{ref1}, \cdots, T_{refN}\} \quad (5)$$

The software computes the simulated response as a sequence of time-amplitude pairs:

$$y_{\sin}(t_{\sin}), t_{\sin} \in \{T_{\sin 0}, T_{\sin 1}, \cdots, T_{\sin N}\} \quad (6)$$

where, some values of t_{sim} may match the values of t_{ref}.

A new time base, t_{new}, is formed from the union of the elements of t_{ref} and t_{sim}. Elements that are not within the minimum-maximum range of both t_{ref} and t_{sim} are omitted:

$$t_{new} = \left\{ t : t_{\sin} \cap t_{ref} \right\} \tag{7}$$

Using linear interpolation, the software computes the values of y_{ref} and y_{sim} at the time points in t_{new} and then computes the scaled error:

$$e(t_{new}) = \frac{(y_{\sin}(t_{new}) - y_{ref}(t_{new}))}{\max\limits_{t_{new}} \left| y_{ref} \right|} \tag{8}$$

Finally, the software computes the weighted, integral square error:

$$f = \int w(t) e(t)^2 dt. \tag{9}$$

When the model has multiple Signal Constraint blocks or vector signals feeding a Signal Constraint block, the tracking objective equals the sum of the individual tracking integral errors for each signal:

$$f = \int w(t) e(t)^2 dt. \tag{10}$$

The above explanation clearly explains how the optimization of parameters is carried out using optimization software and Signal Constraint block. The tuning of the controller using this method having so many advantages but it has some limitations also like optimization software is inbuilt and has no access. Therefore, changes/modifications are not possible and for defining the constraints on signal only GUI of the software can be used. Therefore, the accuracy of the tuning is depending on the user ability for defining the constraint on the signal using GUI. The use of the technique is restricted to platforms where Simulink models can be built and run.

3. AFE NPC 3-LEVEL CONVERTER

Figure 4 shows that there are four devices are required for each phase and clamping diodes are used for clamping in each leg. Three phase supply is given to 3-level converter through inductor. The midpoint of dc link capacitors on the output side and each phase clamping diodes is connected to the neutral on the supply side. Resistance R_1 and R_2 are connected as shown in Figure 4 for loading the converter.

The power devices (S_{x1}, S_{x2}, S'_{x1} and S'_{x2}, x=a, b, c) in each leg are controlled independently and constraints for the connected devices so as to avoid the devices to conduct simultaneously is defined below:

$$S_{xi} + S'_{xi} = 1 \tag{11}$$

where, x = a, b, c and i = 1, 2.

S_{xi} = 1 (switch S_{xi} is turned on) or S_{xi} = 0 (switch S_{xi} is turned off). Hence, the following is the equivalent switching function of the 3-level converter:

$$T_{Sx} = \begin{cases} 1 & if \ S_{x1} = S_{x2} = 1 \\ 0 & if \ S'_{x1} = S_{x2} = 1 \\ -1 & if \ S'_{x1} = S'_{x2} = 1 \end{cases} \tag{12}$$

The above switching function shows that there are three possible modes of operation. The simulation of 3-phase AFE NPC 3-level converter is carried out in MATLAB/SIMULIK environment and results are presented in section 5.

4. DESIGN OF CONTROLLER (UPC)

A controller is required to operate 3-level converter at unity power factor for improved power quality. The Figure 5 shows the control system for operating 3-level converter at unity power factor and termed as unity power factor controller (UPC). The UPC comprises of voltage controller, neutral point potential regulator (NPP) and current controller for which online tuning of PI controllers is explained.

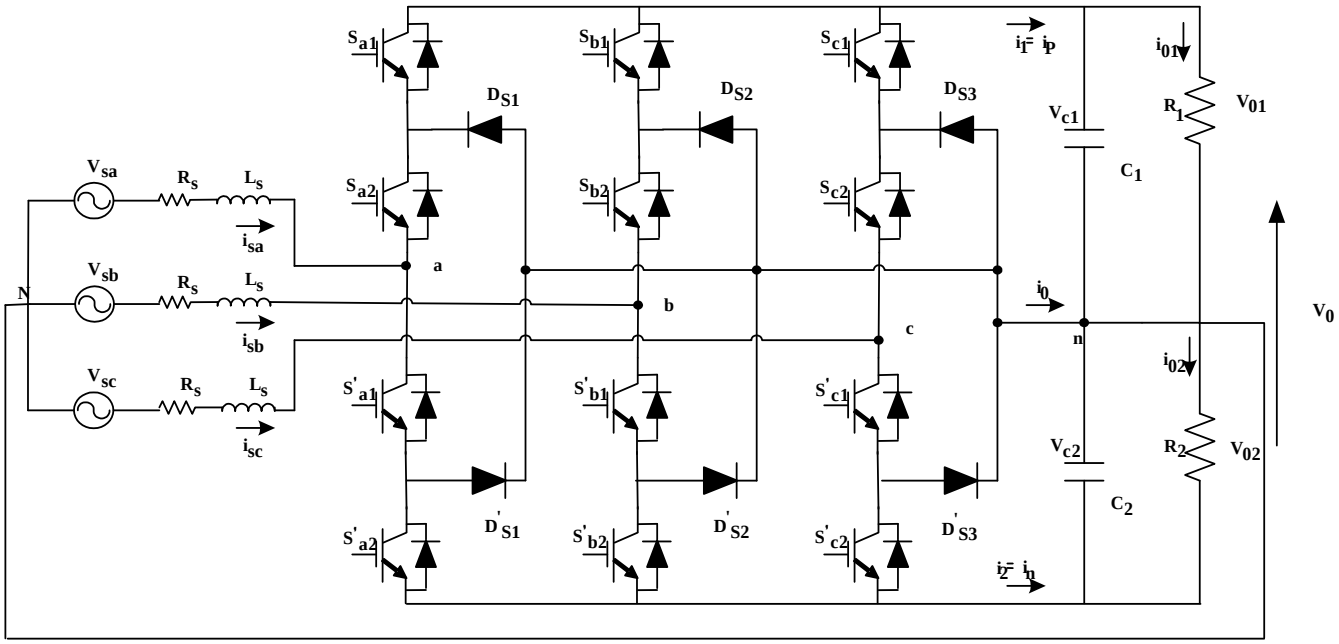


Figure 4. 3-Phase AFE NPC 3-level converter

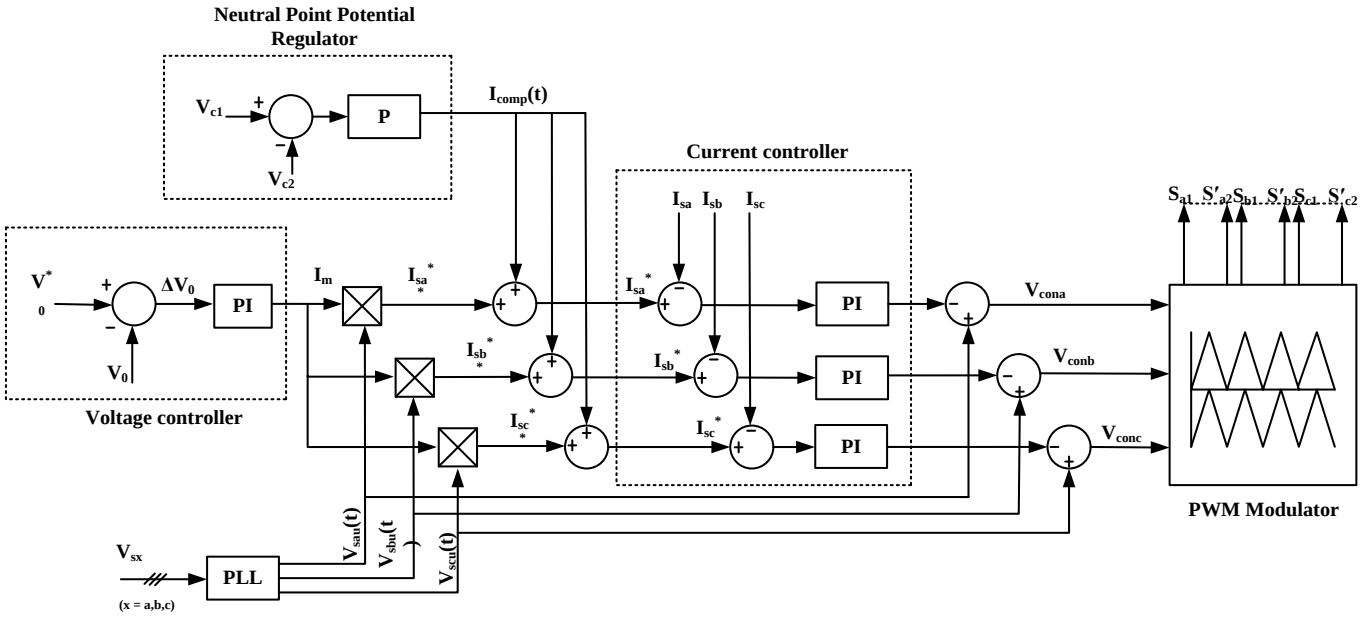


Figure 5. Schematic of Unity Power Factor Controller (UPC)

V_{an}, V_{bn} and V_{cn} are the carrier based unipolar PWM line-to-neutral voltages produced at input side of the converter [14]. Three-unit sinusoidal voltages are generated using the phase locked loop (PLL) circuit which is synchronized with the AC source voltages. The output of the voltage controller comprising of PI controller to minimize the error between two dc link voltages, is the amplitude of the input current commands (I_m) which is multiplied by the generated unit sinusoidal voltages to generate reference supply currents (i_{sa}*, i_{sb}*, i_{sc}*).

The generated reference current is then added to output of NPP regulator. The resultant is compared with actual currents and processed through PI controllers. Control or reference voltages are generated by comparing the output of PI controller and output of PLL [29, 30]. Gating signals are obtained for the devices by comparing these reference/control voltage signals with triangular carrier waves.

4.1 Design of current controller

The line current commands which are defined in equation 13 are compared with sensed actual currents and the error is fed to current controllers which comprises of PI controllers for tracking the source current command.

$$\left.\begin{aligned} i_a^*(t) &= I_m \sin(\omega t) \\ i_b^*(t) &= I_m \sin\left(\omega t - 2\pi/3\right) \\ i_c^*(t) &= I_m \sin\left(\omega t + 2\pi/3\right) \end{aligned}\right\} \quad (13)$$

Neglecting the high-frequency switching terms, source voltage of phase 'a' is define below.

$$V_{sa} = L_{sa}\frac{di_{sa}}{dt} + V_{cona} \quad (14)$$

where, V_{cona} is defined as modulated control signal of PWM based converter from the proposed closed loop current controller. The multi carrier-based SPWM scheme is used for generating the required gating signals as shown in Figure 6 (a & b).

The switching signals for the power switches derived from the SPWM based control system and gating signals can be defined as:

$$T_c = \begin{cases} 1 & if\ v_{cona} > v_{t1} \\ 0 & if\ v_{t1} > v_{cona} > v_{t2} \\ -1 & if\ v_{t2} > v_{cona} \end{cases} \quad (15)$$

Hence switching function can be written as:

$$\left.\begin{aligned} S_{a1} &= \frac{T_c(T_c+1)}{2} \\ S_{a1}^{'} &= 1 - S_{a1} \\ S_{a2}^{'} &= \frac{T_c(T_c+1)}{2} \\ S_{a2} &= 1 - S_{a2}^{'} \end{aligned}\right\} \quad (16)$$

In the first half cycle of the control signals V_{cona}, the line current is controlled by turning on or off the power switch S_{a_1} while the switch S_{a2} is remain turned on during the half cycle for phase 'a'. And in the second half cycle the line current is controlled by turning on or off S_{a2}, and S_{a1} *is* turned off. The phase voltage V_{an} generated on AC side is three level i.e $V_0/2$, 0, and - $V_0/2$.

4.1.1 Tuning of current controller

The performance of a 3-level converter depends on the current control strategy. As compared to open loop converters, following are the advantages of current-controlled PWM (CC-PWM) converter.

- Instantaneous current waveform Control with high accuracy;
- Protection against peak current;
- Dynamic repose is extremely good;
- Effects of Compensation due to change in load parameter (R and L);
- AC-side voltage and DC-bus changes Compensation.

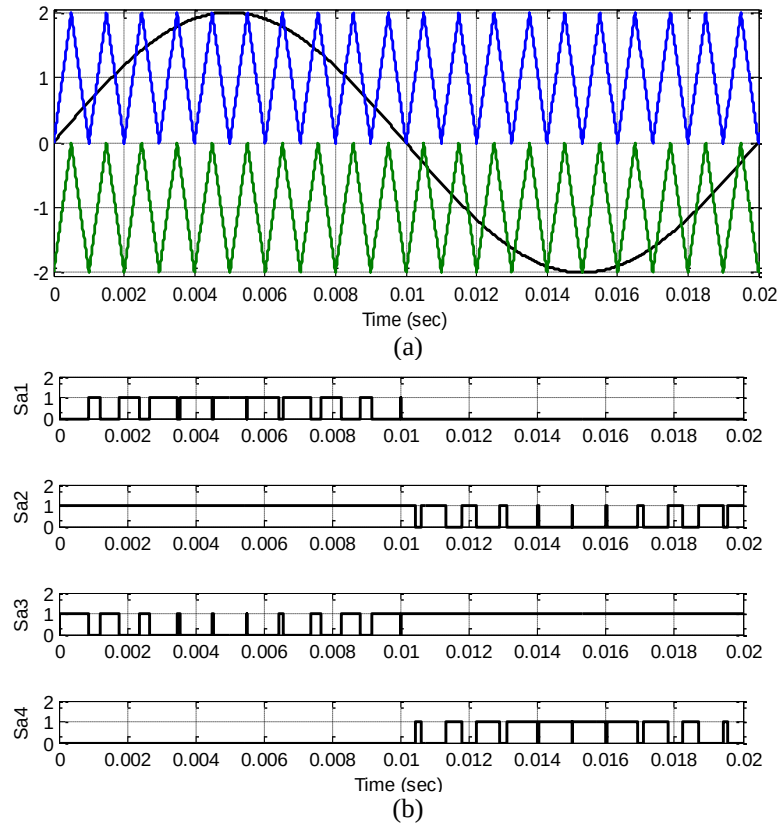


Figure 6. (a) SPWM based control pulses generation; (b) Switching pattern

The PWM based current control techniques can be classified as linear and non-linear controllers [32].

By implementing this concept, it is possible to take the advantages of open loop modulators like space vector PWM, sinusoidal PWM etc. for constant switching frequency with improved power quality and optimal gating pattern. It is also possible to design controller independently with open loop testing with ease. The performance of the multilevel converter depends on the type of reference frame is used for implementing the PI controllers. Literature shows [33] the synchronous reference frame gives better steady state response as compared to stationary reference frame.

Therefore, PI controllers in synchronous reference frame is designed and implemented in this paper. The block diagram of decoupled controller in synchronous reference frame for multilevel rectifier is shown in Figure 7.

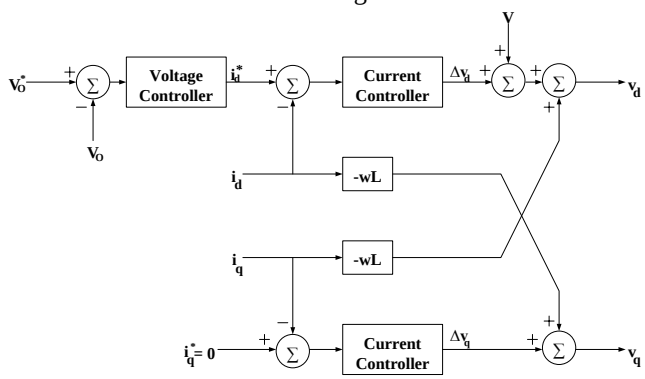


Figure 7. Block diagram of overall control of 3-Phase 3-level converter

The tracking capability of current controller can be improved by decoupling the d *and* q *axes* which reduce the synchronous reference-frame current control plant to a first-order delay.

By doing so it is simple to analysis and allow to derive analytical expressions for the parameters of current controller.

Figure 8 shows the block diagram of simplified current control close loop in the synchronous reference frame.

As shown in the Figure 8, the gains and time-constants of various elements are as follows:

T_s	Sampling time ($T_s = 1/f_s$),
U_L	Disturbance voltage
K_{cp}	PI current controller's Proportional gain
T_{ci}	PI current controller's Time-constant
K_c	Gain of PWM rectifier ($K_c = 1$)
T_F	Time delay of filter
$T_{\mu p}$	Processing time of DSP
T_o	Dead-time ($T_o = T_s / 2$) of Power converter
T_f	Feedback Time delay filter and sampling

The following are the assumptions made

- The cross-coupling effect due to inductance between *d* and *q* axes is neglected.
- Power converter dead-time which includes processing and sampling time is approximated by a first-order inertia element

$$e^{-sT} \approx \frac{1}{1+sT_o} \tag{17}$$

- The sum of small time constants is defined as:

$$\tau = T_{\mu p} + T_o + T_f \tag{18}$$

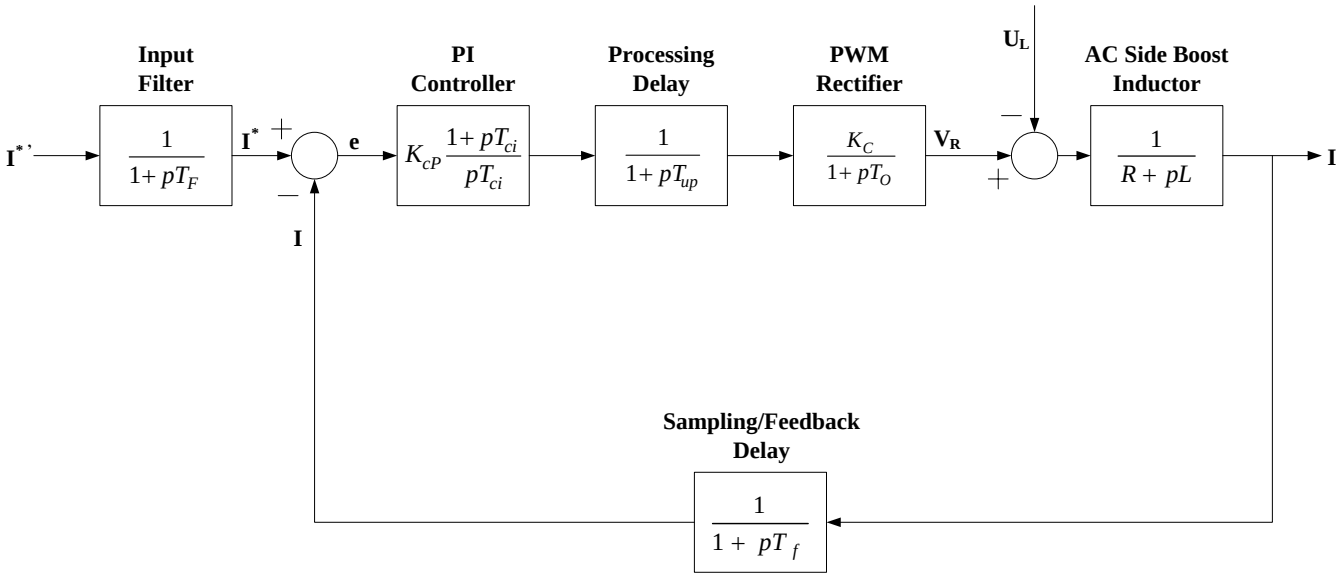


Figure 8. Block diagram of synchronous current controller

The block diagram simplified synchronous current controller is shown in Figure 9 considering U_L=0.

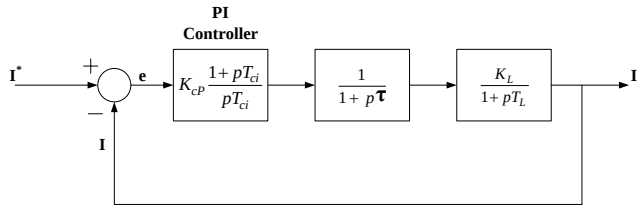


Figure 9. Block diagram of simplified of synchronous current controller

Hence, the open loop transfer function can be expressed as given equation:

$$G_o(p) = K_{cp}\left(\frac{1+pT_{ci}}{pT_{ci}}\right)\left(\frac{1}{1+p\tau}\right)\left(\frac{K_L}{1+pT_L}\right) \tag{19}$$

$$G_o(p) = K_{cp}\left(1+\frac{1}{pT_{ci}}\right)\left(\frac{K_L}{(1+p\tau)(1+pT_L)}\right) \tag{20}$$

And the characteristic equation is defined as:

$$1+G_o(p)\,H_o(p) = 0 \tag{21}$$

$$1+K_{cp}\left(1+\frac{1}{pT_{ci}}\right)\left(\frac{K_L}{p^2\tau T_L + pT_L + p\tau + 1}\right) = 0 \tag{22}$$

The Eq. (22) shows that Synchronous Current Controller is of third order and the optimised parameter for the stable operation of 3-level converter can be found out using accurate available techniques.

Therefore, online tuning of PI controller is used to find the optimised parameter by using Signal Constraint block available in Simulink Design Optimisation library in MATLAB/Simulink environment.

For online tuning the Signal Constraint block is attached to the Simulink model for optimizing the model response to know inputs. Design optimization software in Simulink tunes the parameter of the model as per the applied constraint. The constraints are defined to track the reference signals. The constraints are applicable to vector and matrix-valued ports, in which case the signal bounds and reference signals apply to all entries of the signal/matrix. The optimising methods available in Signal Constraint block are gradient descent, pattern search and simplex search. The gradient descent method with basic gradient type is used to tune current controller for optimum performance of NPC rectifier. The Signal Constraint block is attached to synchronous current controller in the feedback loop as shown in Figure 10.

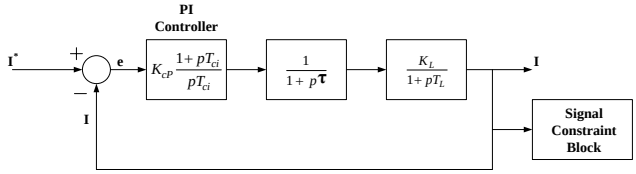


Figure 10. Simplified block diagram of current control loop

The step response of the current controller after completion of optimization process is shown in Figure 11.

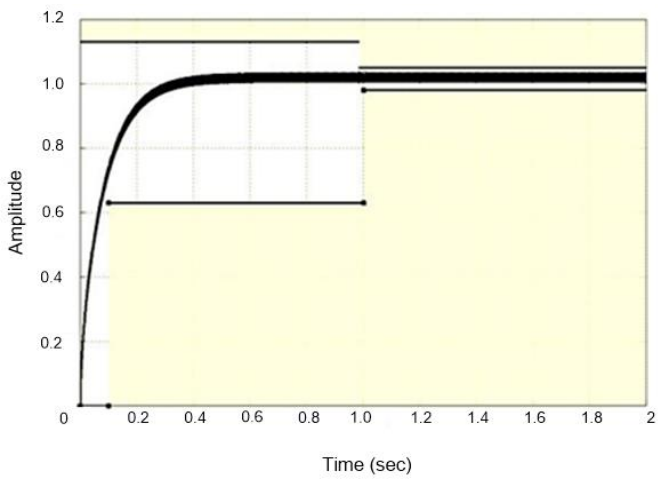


Figure 11. Step response of synchronous current controller

And the optimised proportional gain (K_{cp}) and integral gain (K_{ci}) are found 0.2 and 10 respectively. Thus, the selected transfer function of the PI current controller is given by:

$$0.2\left[\frac{(1+0.02\,p)}{0.02\,p}\right] \tag{23}$$

4.2 Design of voltage controller

A voltage controller is used to maintain the constant DC voltage for balancing of power at AC and DC side. The error of reference voltage and sensed voltage is processed through PI controller to derive amplitude of the line current command (I_m) which is given by

$$I_m = k_p \Delta V_0 + k_i \int \Delta V_0 \tag{24}$$

where, $\Delta V = V^*_0 - V_0$ is voltage error, V^*_0 is the reference DC link voltage and V_0 is sensed DC link voltage. The PLL is used to generate unit sinusoidal voltages can be written as:

$$\left.\begin{aligned} V_{sau}(t) &= \sin \omega t \\ V_{sbu(t)} &= \sin(\omega t + 2\pi/3) \\ V_{scu(t)} &= \sin(\omega t - 2\pi/3) \end{aligned}\right\} \tag{25}$$

4.2.1 Tuning of voltage controller

The voltage controller can be modelled and its block diagram is shown in Figure 12. Following are the various gains and time constants associated with voltage control loop.

T_{dv}	Feedback-loop delay due to sampling, processing time and feedback filter
K_{vp}	Proportional gain of voltage PI controller
T_{vi}	Time-constant of voltage PI controller
C	DC link capacitance

The inner current control loop is modelled with the first order transfer function H_{ci} and given by-

$$H_{ci} = \frac{i}{i^*} = \frac{1}{1+pT_{et}} \tag{26}$$

where, $T_{et} = 2\tau$.

Combining the two smallest time constant in Figure 8 (T_{dv} and 2τ of H_{ci}), the equivalent time constant T_{ev} is obtained as:

$$T_{ev} = T_{dv} + 2\tau \tag{27}$$

The simplified block diagram of Figure 12 is shown in Figure 13.

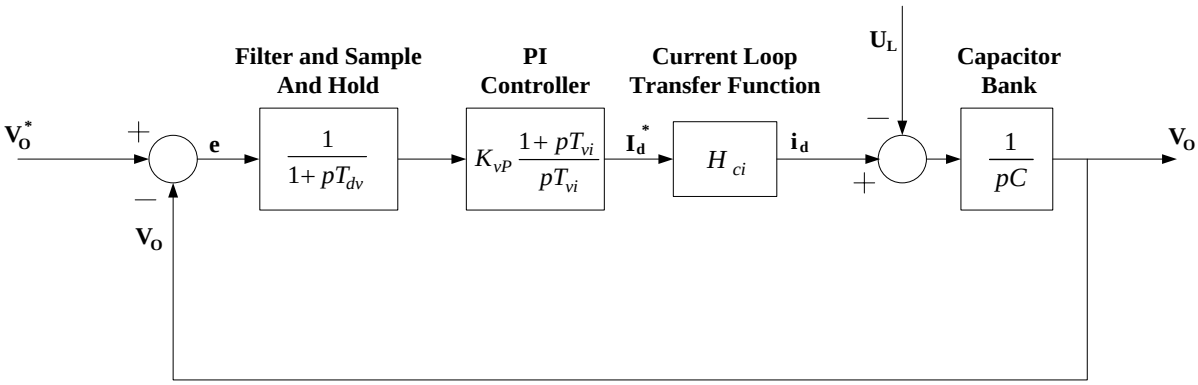


Figure 12. Block diagram of voltage control loop

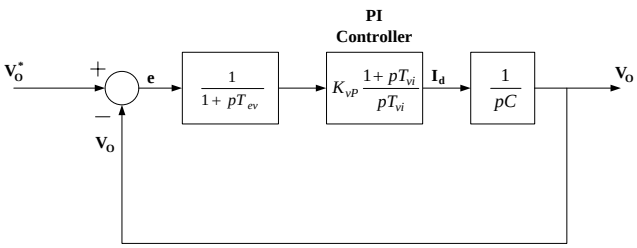


Figure 13. Simplified block diagram of voltage control loop

Assumption is made that the dc link voltage is equal and potential of neutral point is zero. Then the total dc link capacitance is:

$$C = \frac{C_1 (or\, C_2)}{2} \tag{28}$$

And the dc link voltage is evaluated as:

$$V_0 = \frac{1}{C}\int i_c dt = \frac{1}{C}\int i_d dt \tag{29}$$

The open loop transfer function is defined as:

$$G(s) = \left[\frac{K_{vp}(1+pT_{vi}}{pT_{vi}}\right]\left(\frac{1}{1+pT_{ev}}\right)\left(\frac{1}{pC}\right) \tag{30}$$

Hence, the characteristic equation of voltage control loop is given by:

$$1 + G(s)\,H(s) = 0 \tag{31}$$

i.e.

$$1 + \frac{K_{vp}\,(1+pT_{vi})}{pT_{vi}\,(1+pT_{ev})\,pC} = 0 \tag{32}$$

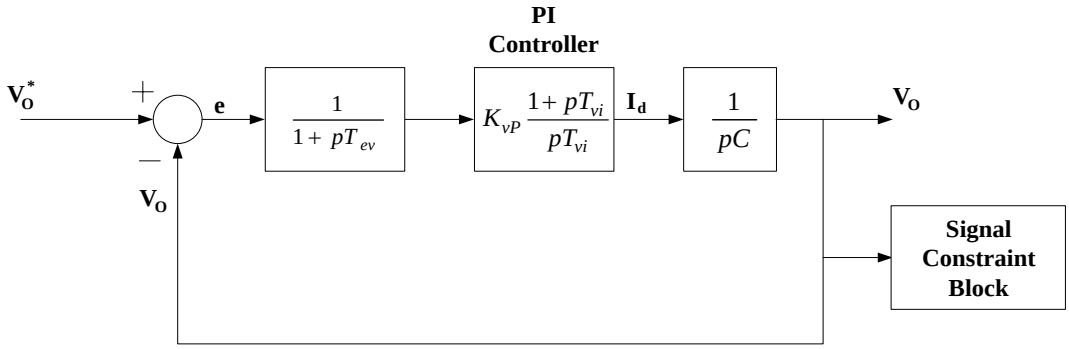


Figure 14. Simplified block diagram of voltage control loop with Signal Constraint block

The characteristic equation shows that the system is of third order. The same Signal Constraint block has been used to evaluate PI controller parameters as explained in Section 4.1.1.

The Signal Constraint block is attached to output of voltage controller in feedback loop which acquires the output dc link voltage for the tuning of PI voltage controller as shown in Figure 14. The output of Signal Constraint block shows different curves for different values of proportional gain (K_{vp}) and integral gain (K_{vi}) of voltage controller as shown in Figure 15. The curve in black is the final step response of voltage controller for optimum values of proportional gain (K_{vp}) and integral gain (K_{vi}) of voltage controller.

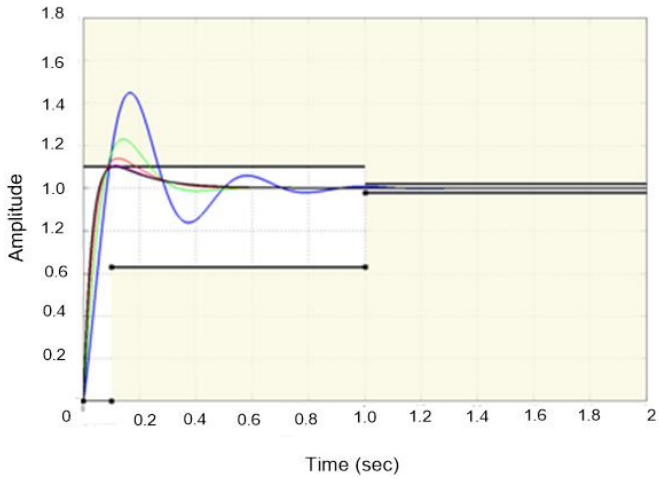


Figure 15. Step response of synchronous voltage controller

The optimised proportional gain (K_{vp}) and integral gain (K_{vi}) for the obtained step response of synchronous voltage controller are 2 and 25 respectively. Hence, the transfer function of the PI voltage controller is given by:

$$2\left[\frac{(1+0.08\,p)}{0.08\,p}\right] \tag{33}$$

4.3 Design of NPP regulator

NPP regulator is designed to control the neutral point potential and it can be done by using general law for the neutral point current as shown under (assuming $C_1 = C_2$).

$$i_1 = C\ \frac{dV_{c1}}{dt} \tag{34}$$

$$i_2 = C\ \frac{dV_{c2}}{dt} \tag{35}$$

Neutral point current is given by:

$$i_0 = -i_1 + i_2 \tag{36}$$

$$i_0 = -C\frac{d(V_{c1} - V_{c2})}{dt} \tag{37}$$

The equation yields,

$$V_{c1} - V_{c2} = -\frac{1}{C}\int i_0 dt + cons\tan t \tag{38}$$

The Eq. (38) shows that i_0 can be used to control NPP.

4.3.1 Tuning of NPP regulator

For tuning the NPP controller the procedure will remain the same as explained in 3.2.1. And the optimal parameters for tuned NPP controller are 2 for defined constraints.

5. SIMULATION RESULTS

In this section, simulation results are presented based on designed UPC (Figure 5) for AFE NPC converter (Figure 6). The simulation study is carried out to evaluate the performance of AFE NPC 3-level converter under transient and steady state condition with online tuned parameters for UPC using Signal Constraint block of Simulink Design Optimisation library in MATLAB/Simulink environment. The simulation parameters and selected UPC parameters are given in Table 2 and Table 3 respectively.

Table 2. Simulation parameters for 3-level converter

RMS Phase Voltage	Vsa	3810 V
Inductor	Ls	30mH
Resistance on AC Side	R	0.8 Ω
Voltage DC Side	V_{dc}	11000 V
Capacitance	C_1/ C_2	100000 µF
Load Resistance	$R_1 \parallel R_1$'	60 Ω ‖ 60 Ω
	$R_2 \parallel R_2$'	60 Ω ‖ 60 Ω
Switching Frequency	f_c	2050 Hz

The unity power factor operation of converter is the important criteria for the evaluation of performance of the converter. The result shown in Figure 16, confirms that the PI controllers of current controller are accurately tuned as supply

current is in phase with supply voltage which is primary requirement of the UPC. The harmonic profile of phase 'a' line current is shown in Figure 17 and THD is well below the limit defined in IEEE519 standard i.e. 2.39%.

Table 3. Selected tuned controller for the converter

Current Controller Parameters	
K_{cp}	0.2
K_{ci}	10
Voltage Controller Parameters	
K_{vp}	2
K_{vi}	25
NPP Regulator Parameters	
K_{np}	2

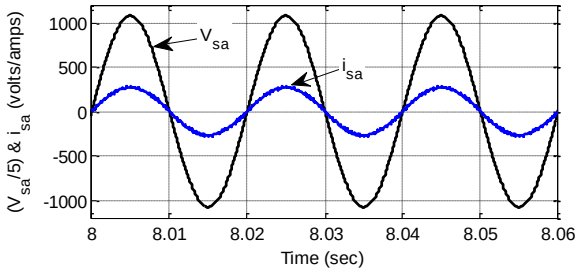


Figure 16. Source voltage (V_{sa}) and line current (i_{sa}) of Phase 'a'

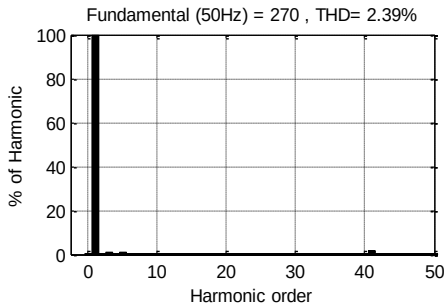


Figure 17. Harmonic spectrum of line current (i_{sa})

5.1 Steady state performance

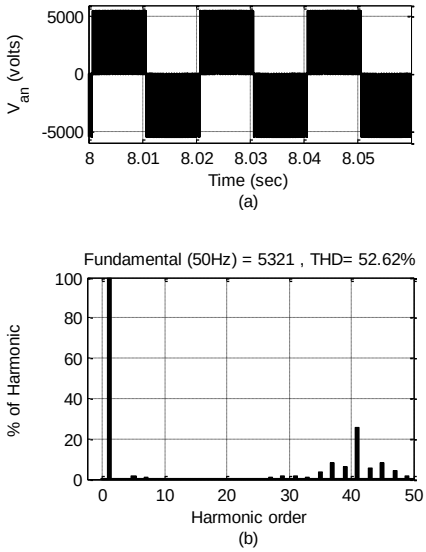


Figure 18. AC side (a) phase voltage (V_{an}) (b) Harmonic spectrum of phase voltage (V_{an})

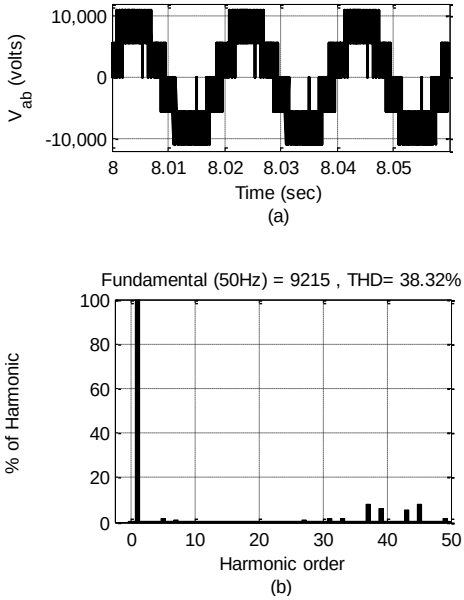


Figure 19. AC side (a) Line-Line voltage (V_{ab}) (b) Harmonic spectrum of line-line voltage (V_{ab})

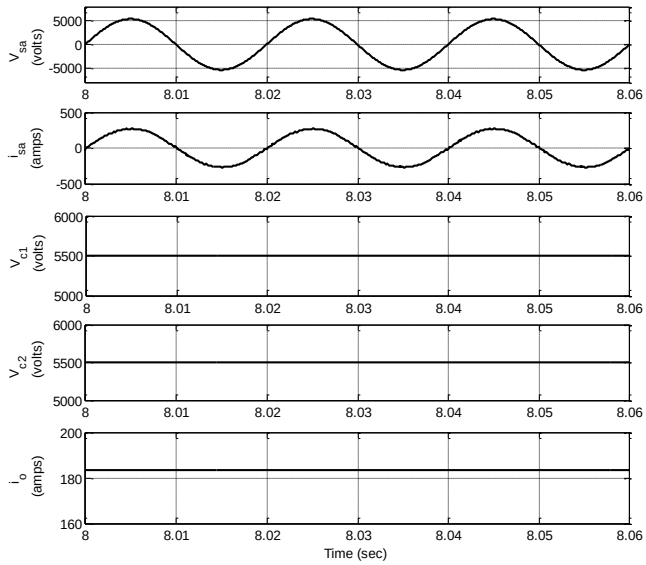


Figure 20. Voltage (V_{sa}), current (i_{sa}), dc link capacitor voltages (V_{c1} and V_{c2}) and load current (i_0) under steady state condition

Another important performance index of 3-level converter is performance of converter under steady state. Therefore, AC side phase voltage and its THD profile and AC side line voltage with its THD profile has been observed and shown in Figure 18 and Figure 19 respectively. Also, the steady state phase voltage (V_{sa}), Line current (i_{sa}), dc link capacitor voltages (V_{c1} and V_{c2}) and load current (i_0) are shown in Figure 20. The result shows satisfactory operation of the converter under steady state condition.

The results shown in these Figures clearly show the stable operation of AFE NPC 3-level under steady state.

5.2 Performance under transient condition

The real testing of the PI controllers of UPC is the satisfactory performance of the converter under transient condition. Therefore, the dynamic behaviour of 3-level

converter for tuned PI controllers has been observed under transient conditions.

DC link capacitor voltages V_{c1} and V_{c2} and Phase 'a' source current (i_{sa}) is shown in Figure 21. The result shows that V_{c1} and V_{c2} settled down quickly (within 10 cycles) and i_{sa} remains sinusoidal after sudden increase in load current.

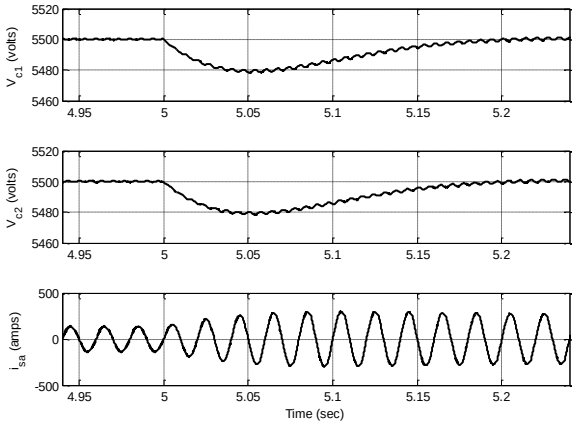


Figure 21. Capacitor Voltages (V_{c1} and V_{c2}) and current (i_{sa}) for increase in load at t = 5 sec

The dynamic response of the converter when load is suddenly reduced is also analysed. Figure 22 shows V_{c1} & V_{c2} and i_{sa} when load is reduced and it is observed that it settled down within 10 cycles due to proper tuning of PI controllers in the current and voltage controller.

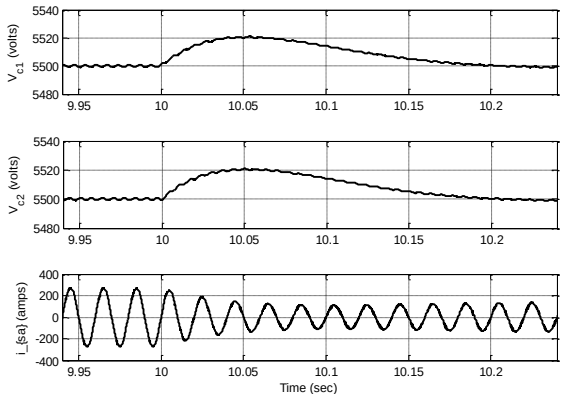


Figure 22. Capacitor Voltages (V_{c1} and V_{c2}) , and current (i_{sa}) for decrease in load at t = 10 sec

The simulation results under transient condition validate the optimised tuning parameters of PI controllers of UPC.

5.3 Neutral Point Potential (NPP) control

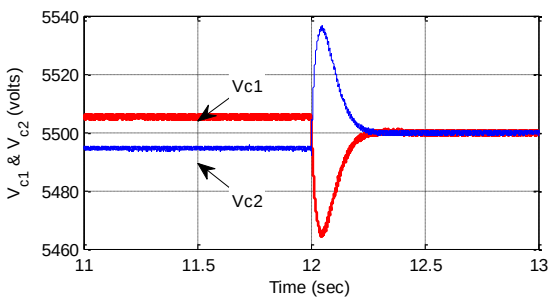


Figure 23. DC link capacitor voltages (V_{c1} & V_{c2}) under unbalanced load

The working of NPP is also verified through simulation by introducing the unbalance load. The V_{c1} & V_{c2} are shown in Figure 23 which shows the effective working of NPP regulator when it is included at t=12 sec.

6. EXPERIMENTAL RESULTS

A prototype is developed in the laboratory for validating the simulation results. The developed experimental setup comprises of following parts:

1. Power circuit of AFE NPC 3-level converter (IGBT rectifier and gate driver circuit),
2. Measurement of system parameters such as supply voltages, line currents and dc link voltages,
3. Implementation of control scheme through dSPACE DS1103 real time controller,
4. Interfacing DS1103 Master Bit I/O with the associated hardware.

Real time implementation is done for performing the experimentation on developed prototype. The parameters chosen for experimentation are given in Table 4.

Table 4. Experimental parameters for NPC AFE 3-Level converter

RMS Line Voltage	V_{LL}	50 V
Inductor (source)	L_s	7.73mH
Resistance (AC Link)	R	0.4 Ω
DC Link Parameters		
Voltage (DC Link)	V_{dc}	80 V
DC Link Capacitors	C_1 and C_2	2200 µF
Load Parameters		
Loading Resistances	(R_1 and R_2)	15 Ω
Switching Frequency	f_c	2050

The experimental results show that supply voltage and current and in phase (Figure 24) which validate the simulation results. The harmonic spectrum of i_{sa} and V_{ab} shown in Figure 25 (a & b) and shows that the THD in supply current is only 2.4% and verify the simulation results.

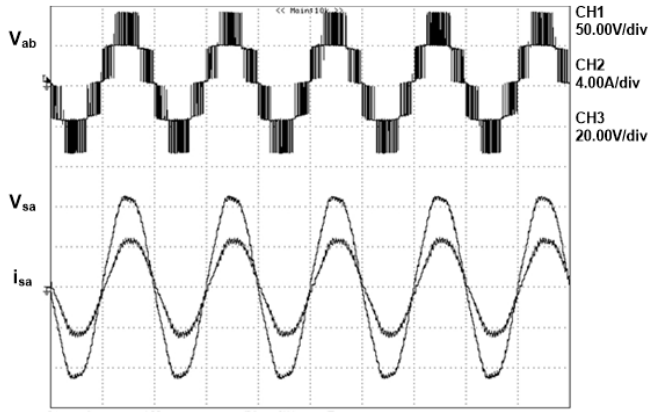
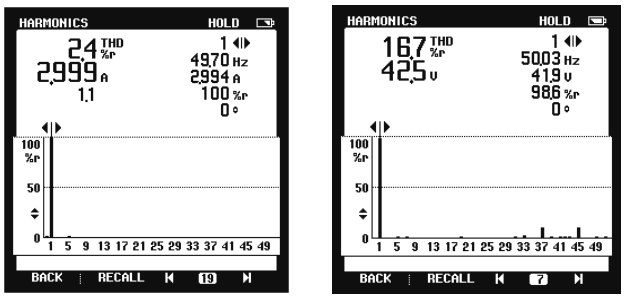


Figure 24. Voltage (V_{ab}) at supply end, phase voltage (V_{sa}) and current (i_{sa})
X - axis: Time – 10ms/div, Y axis: V_{ab} - 50 V/div, V_{sa} – 20V/div and i_{sa} – 4A/div



(a) (b)

Figure 25. Harmonic spectrum of (a) Line current (i_{sa}) and (b) Line voltage harmonic spectrum at supply end (V_{ab})

6.1 Steady state analysis

The phase voltage (V_{an}) at supply end is shown in Figure 26 under steady state condition.

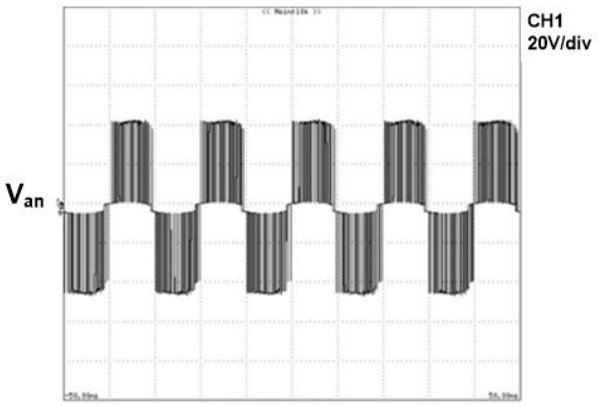


Figure 26. Voltage (V_{an}) at supply end of 3-level converter under steady state condition
X - axis: Time –10ms/div, Y - axis: V_{an} - 20 V/div

The dc link capacitors voltages V_{c1} and V_{c2} under steady state condition are shown in Figure 27. This validates effective working of UPC maintaining desired dc link voltage.

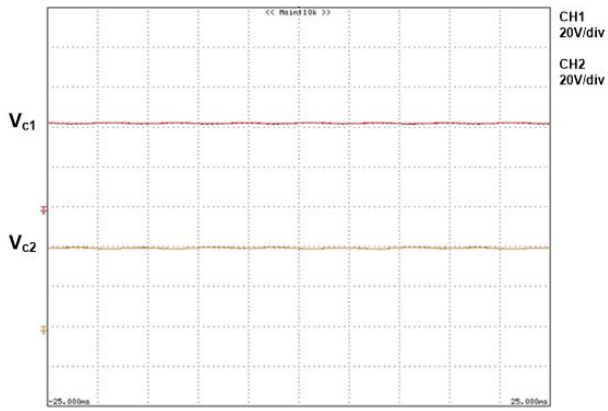


Figure 27. Capacitor voltages (V_{c1} and V_{c2}) of 3-level converter under steady state condition
X axis: Time- 10ms/div, Y axis: V_{c1} and V_{c2} - 20 V/div

6.2 Performance under Transient Condition

For validating the dynamic response of the converter under transient condition, the load is suddenly changed and response of V_{c1} and V_{c2} and i_{sa} has been recorded (Figure 28 and Figure 29). The results confirmed that the PI controllers in UPC is effectively tuned and able to regulate dc link voltage quickly at desired value under transient condition. Therefore, the tuned parameters obtained from the optimization software are the required parameters for the real time implementation of the proposed system.

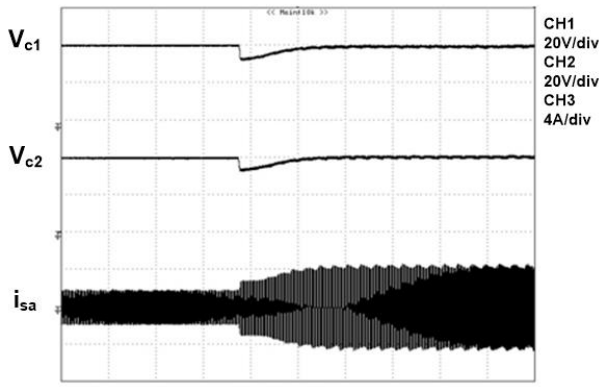


Figure 28. Capacitor voltages (V_{c1} and V_{c2}) and current (i_{sa}) when load is increased
X - axis: Time – 1s/div, Y - axis: V_{c1} and V_{c2} - 20 V/div, i_{sa} – 4 A/div

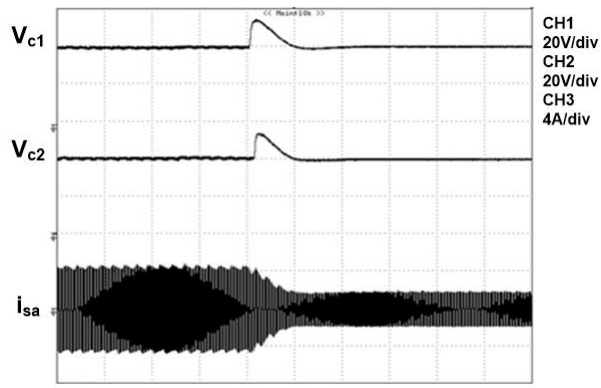


Figure 29. Capacitor voltages (V_{c1} and V_{c2}) and current (i_{sa}) when load is decreased
X - axis: Time – 1s/div, Y- axis: V_{c1} and V_{c2} - 20 V/div, i_{sa} – 4 A/div

6.3 NPP control

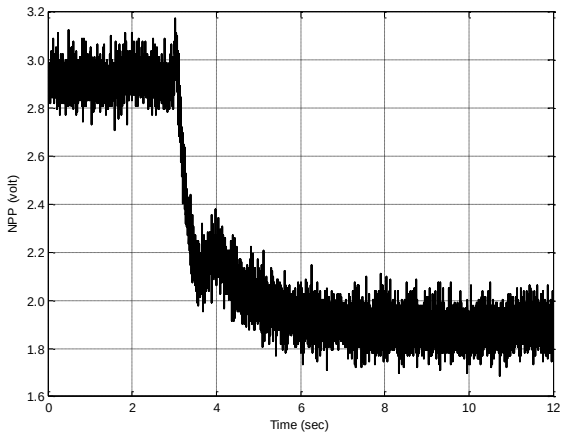


Figure 30. NPP variation in NPC AFE 3-level converter

A neutral point potential regulator is used in UPC to control the NPP variations. To verify its effective working experimentally, NPP regulator has been included in UPC. The NPP variations are shown in Figure 30. The experimental result also confirms that when NPP regulator is included in the controller, the variations has been considerably reduced.

7. CONCULSION

Design of unity power factor controller is presented in this paper for active front end neutral point clamped 3-level converter. A simplified and accurate online tuning of PI controllers is derived and implemented for AFE NPC 3-level converter. Complete modelling of UPC controller is presented and simulation is carried out for the verification of derived online tuning method of PI controllers in UPC. The simulation result with online tuning of PI controllers in UPC confirms the satisfactory performance of AFE NPC 3-level converter under steady state and transient condition. A laboratory prototype is also developed for implementation of UPC with online tuning for AFE NPC 3-level converter. Experimental results validate the simulation results and confirm the easier and effective implementation of proposed online tuning method in real time application.

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